28/4/2019

UNIT-4

8085 MICROPROCESSOR Interfacing (U6)

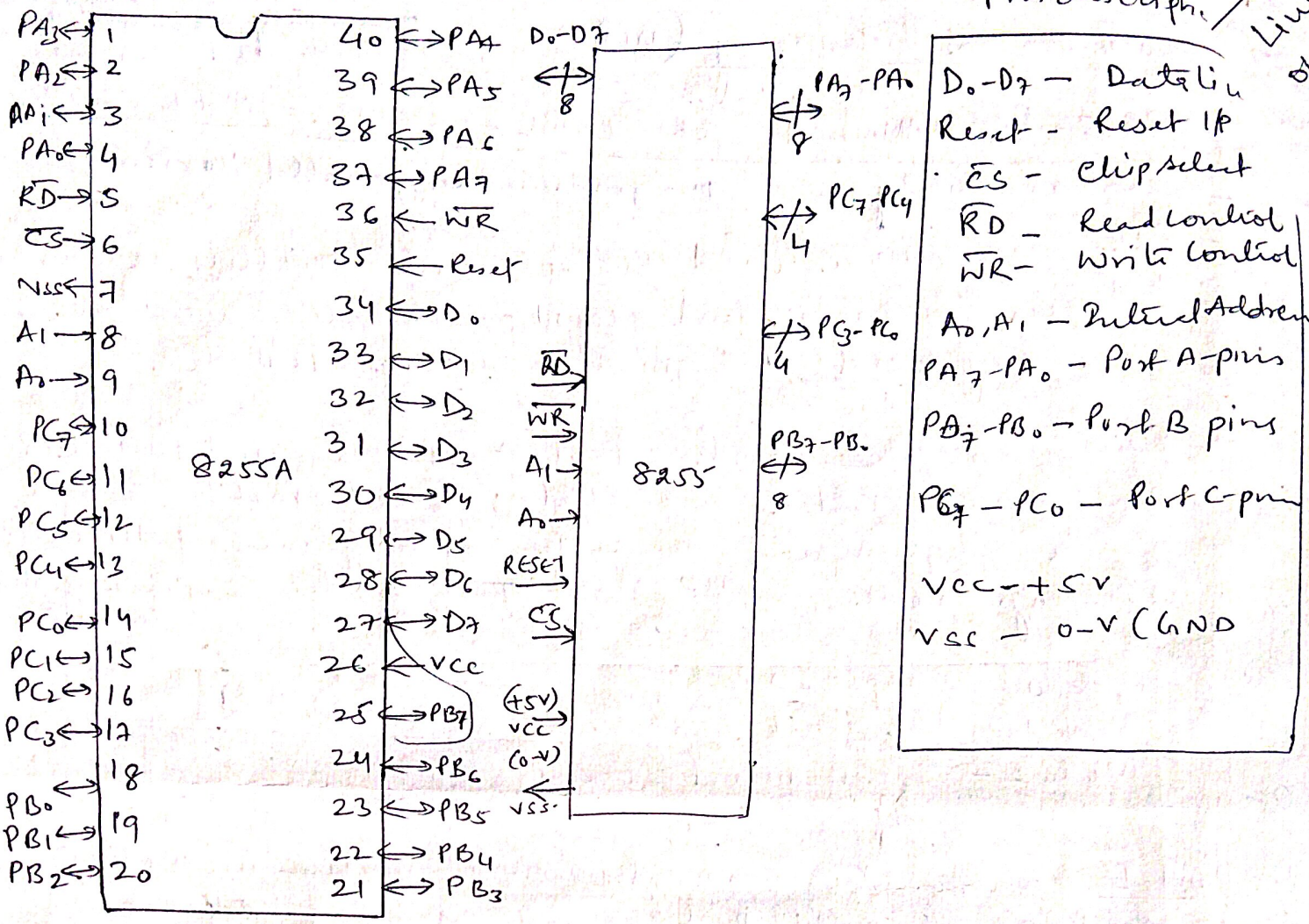
8255 has 24 I/O grouped in two 8bit Parallel port A & B. Remaining 8bits in Port C. Group with 4bit - C_U and C_L.

8255 - PROGRAMMABLE PERIPHERAL INTERFACE - INTEL 8255

- 8255 is widely used, programmable, parallel I/O device.
- 8255 is a device used to implement Parallel data transfer between Processor and slow peripherals devices like ADC, DAC, Keyboard, 7 Segment display, LCD etc.
- 8255 has three ports: Port-A, Port B and Port-C. The ports A and Port B are 8bit Parallel Ports. The Port-A can be programmed to work in any one of three operating modes as I/P or O/P ports. The 3 operating modes are:-
  - Mode 0 - Simple IO Port
  - Mode 1 - Handshake IO port
  - Mode 2 - Bidirectional IO port.
- Port B can be programmed to work either in mode 0 or mode 1 as I/P or O/P port.
- Port C - pins (8pins) have different assignment depending on the mode of port A and B. If Port A and Port B are programmed in mode 0, then Port C can perform one of the following functions:-
  1) 8bit Parallel port in mode-0 for I/P or O/P
  2) Two no. of 4bit parallel port in mode 0 for I/P or O/P.
  3) Individual pin of port C can be set or reset for various control Applications.
- Port A — Programmed in mode 1 / mode 2 and Port-2 is programmed in mode 1 then port C are used for Handshake signals.

PINS, SIGNALS and Internal Block Diagram of 8255:-

It has 40 pins and requires a single +5 volt power supply. The Internal Block diagram and Pin diagram is shown on Next page.



PIN DESCRIPTION OF 8255

- Ports are grouped as Group A and Group B.
- Group A - Has port A, port C (upper) and its control unit.
- Group B - Comprises of Port B, port C-lower and its control unit.
- The Read/Write control logic requires six control signals.

1) RD (Read) - This control signal enables Read op^n. When signal is low, the MP reads data from a selected IO port of 8255.

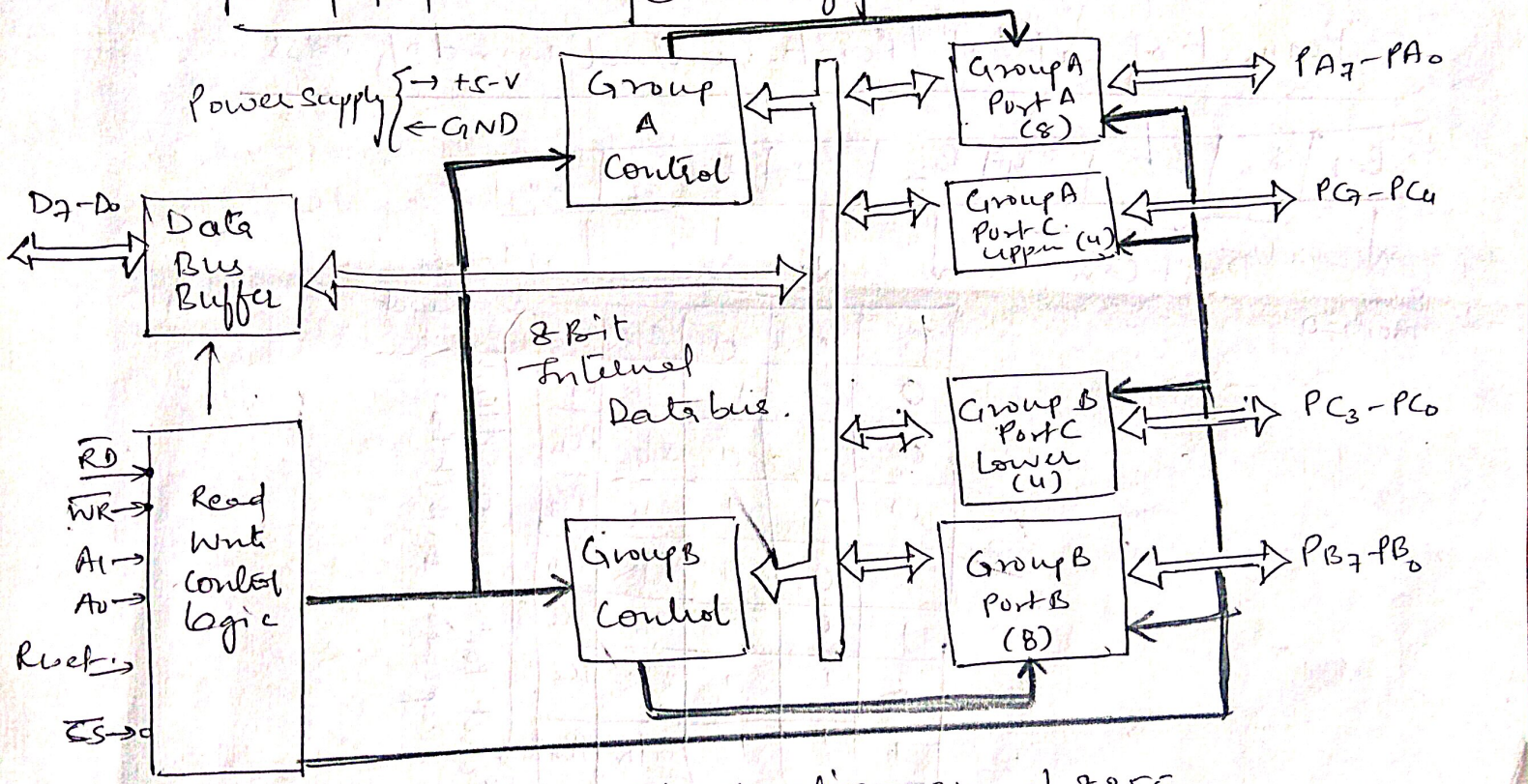
2) WR (Write) - Control signal enables write operations. When signal goes low, MP writes into the selected I/O ports or control Register.

3) RESET: An active high signal, It clears the control register and set all ports in the I/P mode.

$\overline{CS}$, A_0 and A_1 - These are device select signals. The address lines A_0, A_1 of 8255 connected to any two Address lines of Processor to provide internal addresses. The A_0 and A_1 select any 4 internal devices. 8255 will remain in High Impedance state if the signal I/P to $\overline{CS}$ is High.

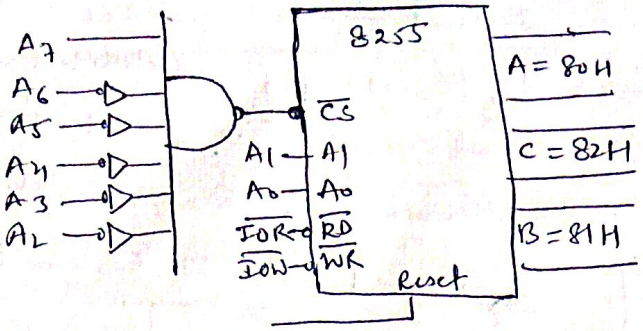
Internal address		Device Selected
A_1	A_0	
0	0	Port A
0	1	Port B
1	0	Port C.
1	1	Control Reg

$\overline{CS}$	A_1	A_0	Selected
0	0	0	Port A
0	0	1	Port B
0	1	0	Port C
0	1	1	Control Reg
1	X	X	8255 not selected



Internal Block diagram of 8255.

Example - The port addresses are determined by the $\overline{CS}$, A_0 and A_1 lines. The $\overline{CS}$ line goes Low when A_7 = 1 & A_6 through A_2 are at Logic 0. When these signals are combined with A_0 & A_1. The port addresses range from 80H to 83H.



CS						Hex address			Port
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	0	0	0	0	0	0	0	= 80H	A
1	0	0	0	0	0	0	1	= 81H	B
1	0	0	0	0	0	1	0	= 82H	C
1	0	0	0	0	0	1	1	= 83H	Control Register

Port Address – In Memory mapped I/O, when address line A_{15} is High, $\overline{CS}$ is enabled.

Port A = 8000H ($A_1=0, A_0=0$)
Port B = 8001H ($A_1=0, A_0=1$)
Port C = 8002H ($A_1=1, A_0=0$)
Control Reg = 8003H ($A_1=1, A_0=1$)

Format of Bit Set / Reset Control word of 8255

B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0

B_7 → BSR mode = 0
B_6, B_5, B_4 → Don't Care
B_3, B_2, B_1 → Select Port-C Pin to Set/Reset Depending on bit B_0
B_0 → 1 = Set, 0 = Reset

0	0	0	S/R	PC_0
0	0	1	S/R	PC_1
0	1	0	S/R	PC_2
0	1	1	S/R	PC_3
1	0	0	S/R	PC_4
1	0	1	S/R	PC_5
1	1	0	S/R	PC_6
1	1	1	S/R	PC_7

Control word

D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 = 83H

- D_7 = 1 → I/O function
- D_6 D_5 = 0 0 → Port A in Mode 0
- D_4 = 0 → Port A = O/P
- D_3 = 0 → Port C (U) = O/P
- D_2 = 0 → Port B in Mode 0
- D_1 = 1 → Port B = I/P
- D_0 = 1 → Port C = I/P

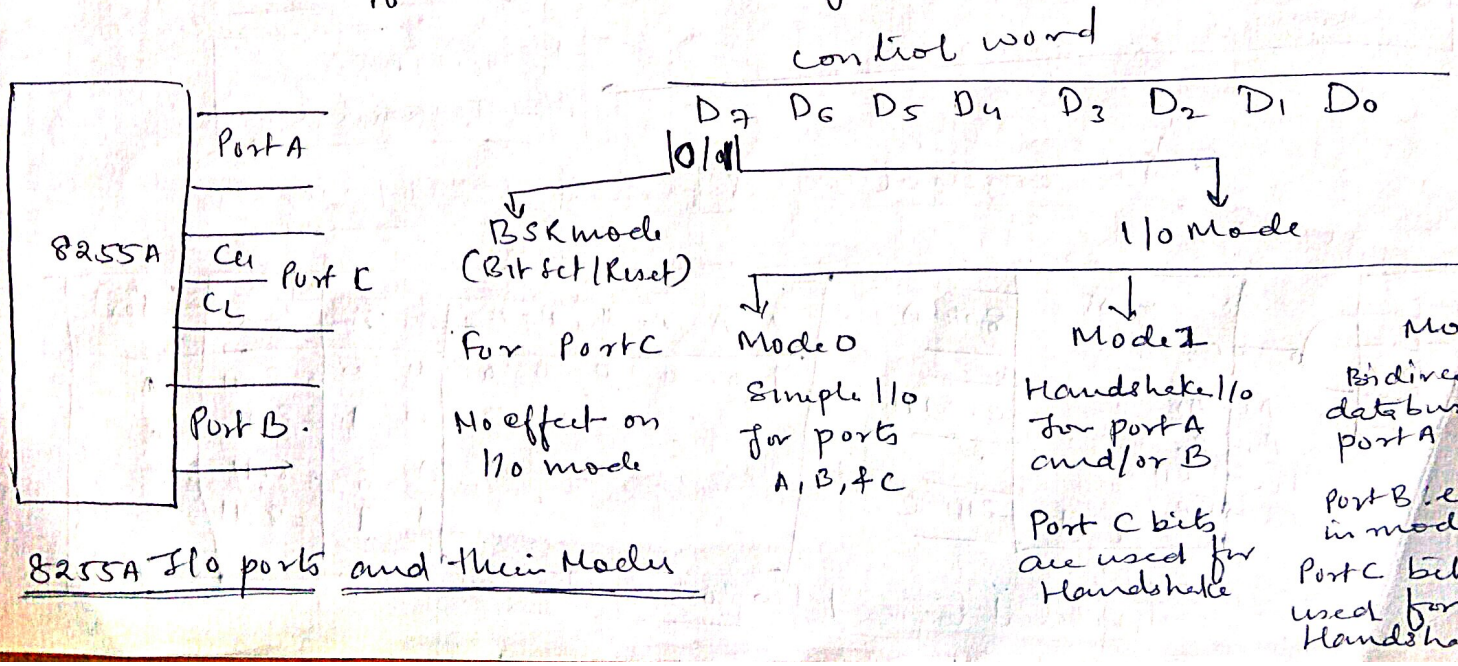
8255 has 24 I/O pins that can be grouped in two 8bit parallel ports: A and B, with remaining eight bits as Port C. The eight bits of port C can be used as individual bits or be grouped in two 4 bit ports: Cupper (CU) and Clower (CL)

- 8255 classified according to two modes :- BSR mode & I/O Mode. The BSR (Bit Set/Reset) mode is used to set or Reset the bits in Port C.

- I/O modes is fullin divided into three modes: Mode 0, mode 1 and mode 2.
  - → In Mode 0 - All ports function as simple I/O ports.
  - → In Mode 1 - Is handshake mode where by port A and/or B use bits from port C as Handshake signals. In the Hand shake mode, two types of I/O data transfer can be implemented : Status Check and Interrupt
  - → In Mode 2 - Port A can be set up Bidirectional data transfer using Handshake signals from port C and port B can be set up either in mode 0 or Mode 1.

Block diagram :- 8255A

Two 8bit ports (A and B), two 4bit ports (CU and CL), the data bus Buffer, and Control logic.



8255A I/O ports and their Modes

Control Word - The content of control Register called The control Word - This register can be accessed to write a control word when A_0 and A_1 are logic 1.

Bit D_7 specifies either I/O function ($D_7 = 1$) or The BSR function ($D_7 = 0$) (Port C operation)

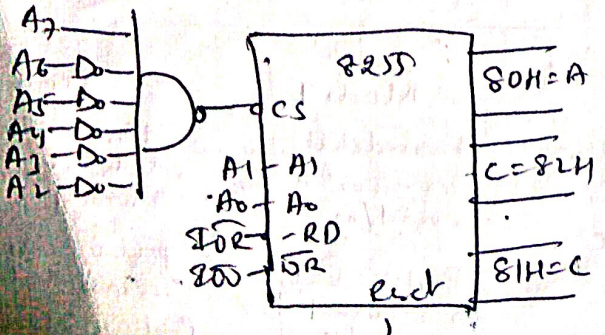
Mode 0 - Simple I/P or O/P

Control Word

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

- D_0 → Group B: Port C_L (PC_3-PC_0): 1 - I/P, 0 - O/P
- D_1 → Group B: Port B: 1 - I/P, 0 - O/P
- D_2 → Group B: Mode Selection: 0 - Mode 0, 1 - Mode 1
- D_3 → Group A: Port C_U (PC_7-PC_4): 1 - I/P, 0 - O/P
- D_4 → Group A: Port A: 1 - I/P, 0 - O/P
- D_5, D_6 → Group A: Mode Selection: 00 - mode 0, 01 - mode 1, 1X - mode 2
- D_7 → 1 - I/O Mode, 0 - BSR mode

8255 Control Word format for I/O mode

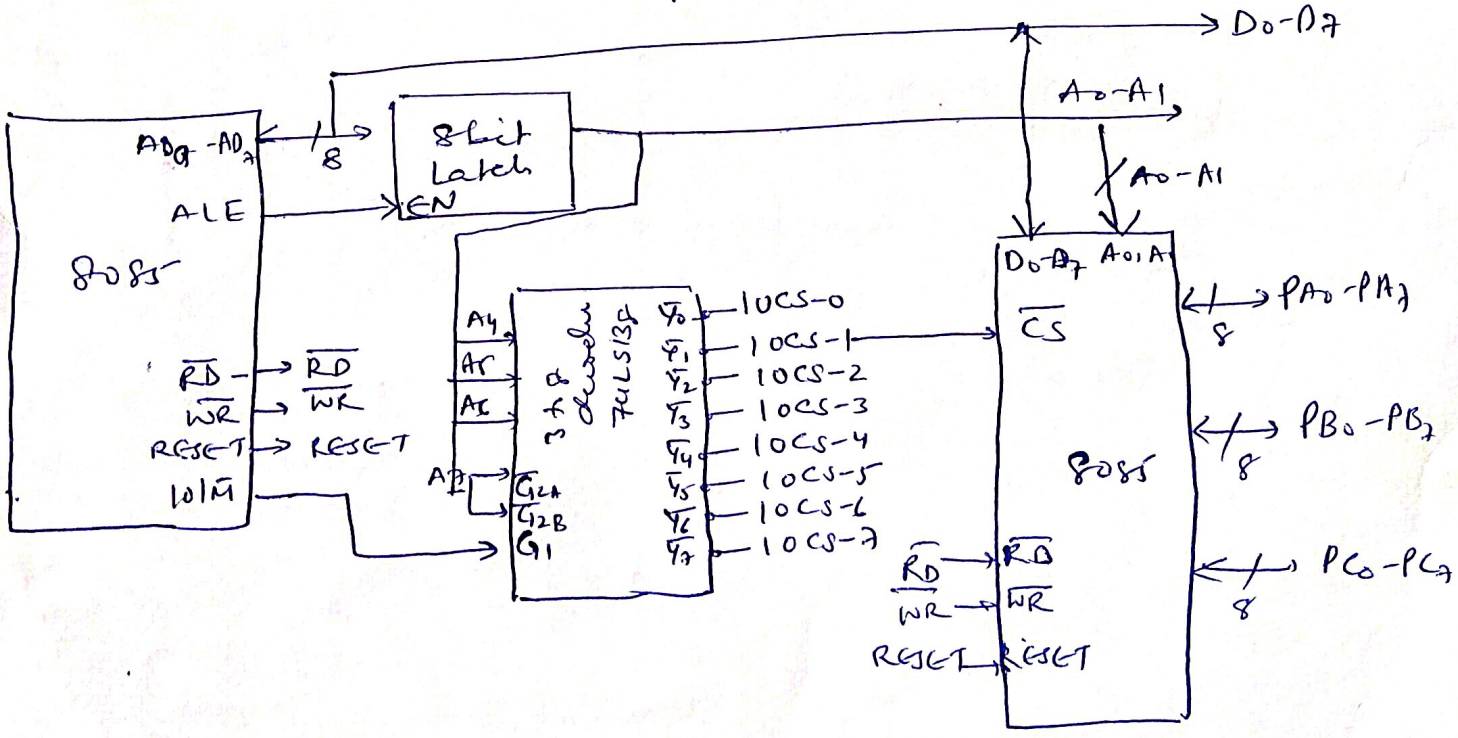


8255 Chip select logic and I/O port Address

CS								Hex Code	Port
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	0	0	0	0	0	0	0	= 80H	A
						0	1	= 81H	B
						1	0	= 82H	C
						1	1	= 83H	Control Register

INTERFACING OF 8255 WITH 8085 PROCESSOR

- 8255 can be either Memory-Mapped or I/O Mapped in the System.
- The 8255 is I/O Mapped in the system.
- The chip select signals for I/O Mapped device are generated by using a 3-8 decoder.
- The Address line A_4, A_5, A_6 are decoded to generate chip select signals (IOCS-0 to IOCS-7) and the chip select IOCS-I is used to select 8255.
- Address line A_7 and Control signal IO/$\overline{M}$ are used as enable for the decoder.
- Address line A_0 & A_1 of 8085 is connected to A_0 & A_1 of 8255 to provide internal Address.
- The I/O address allotted to Internal device of 8255 are.
- The Data line D_0-D_7 are connected to D_0-D_7 of the Processor to achieve parallel data transfer.



8259 - PROGRAMMABLE INTERRUPT CONTROLLER :-

10/4/2017

- It manage 8 interrupt according to the Instruction written into its control Registers.
- To provide 8 Interrupt pin on the processor in place of one INTR (8085) pin
- Resolve 8 levels of Interrupt Priority in a variety of modes, such as fully nested mode, Automatic rotation mode & Specific rotation mode.
- Mask each Interrupt request
- Read the status of pending interrupt, In-Service interrupts and masked Interrupts.
- Set up to work with either the 8085 MP mode or 8086/8088 MP.

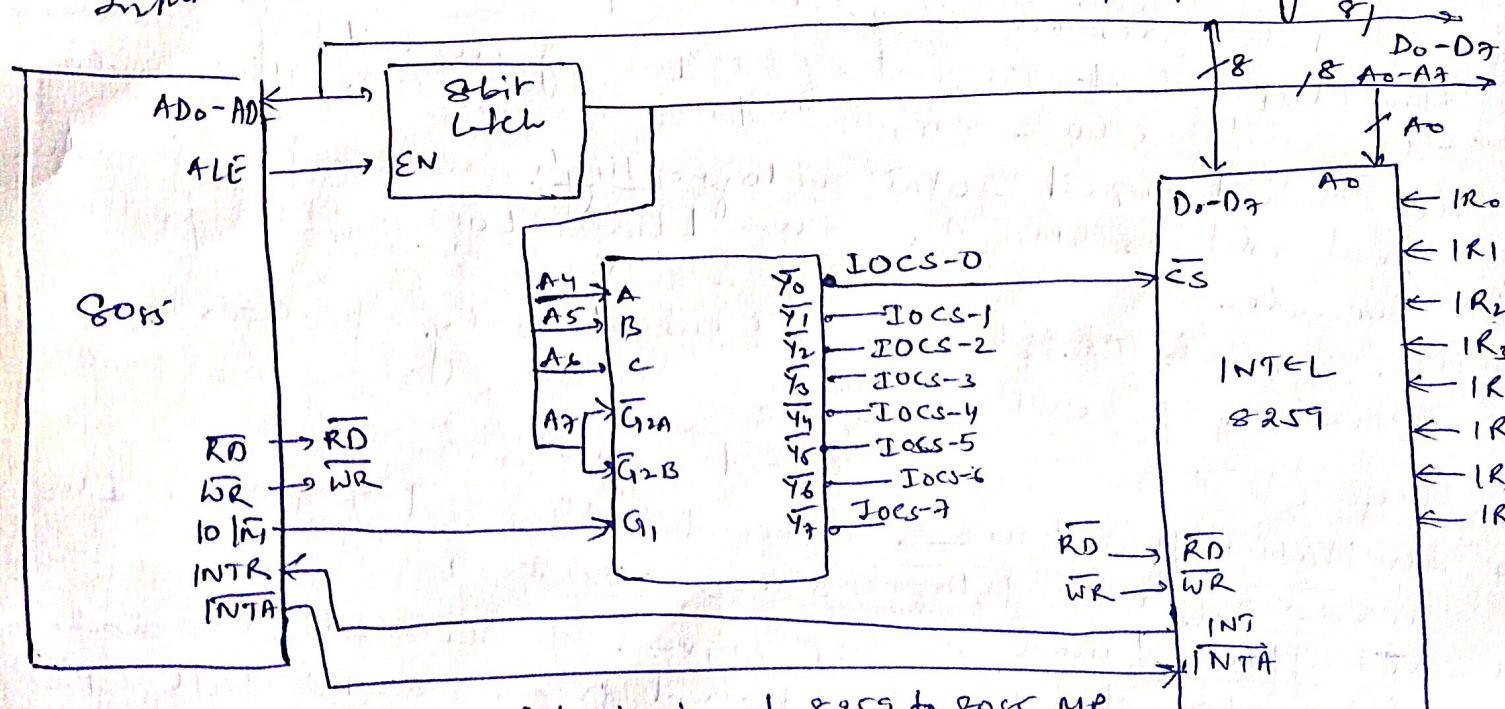
Interfacing 8259 with 8085 MP :-

- 8259 is 28 pin IC packed in DIP.
- It has two internal addresses $A_0 = 0, A_0 = 1$
- It can be either Memory mapped or IO mapped in the system.
- The Interfacing of 8259 to 8085 shown

* The lower order data bus line $D_0 - D_7$ are connected of 8259.
* The address line A_0 of the 8085 MP is connected to A_0 of 8259 to provide the internal address.
* 8259 requires one chip select signal.
* The chip select signal of 8259 is generated by 3 to 8 decoder the address line A_4, A_5 and A_6 are used I/P of decoder.
* The control signal IO/$\overline{M}$ is logic High value for decoder and address line A_7 is used logic LOW value for decoder.
* The signals $CAS_0 - CAS_2$ are used only in cascade Operation of 8259's.
* The $\overline{SP}/\overline{EN}$ pin can be used as I/P or O/P signal.
* In Non-buffered mode it used as I/P signal and Logic 1 in Master 8259 and logic 0 in Slave 8259
* In buffered mode as O/P signal to disable the data buffer which data is transferred from 8259A to the CPU

After 8259 Initialized, the following Sequence of events occurs when one or more request lines go High.

1) IRR stores the requests
2) Priority Resolver Checks three registers :- The IRR for Interrupt request, The IMR for masking bits and ISR for interrupt Request being served. It resolves the priority and set the INT High.
3) MPU Acknowledge the Interrupt by sending $\overline{INTA}$.
4) After $\overline{INTA}$ is received, the priority bit in the ISR is set to indicate which Interrupt line is being served, Corresponding bit in IRR is reset to indicate that the requested is accepted. Then opcode CALL instruction is placed data on data bus.
5) When the MPU decodes the CALL Instruction, it places two more $\overline{INTA}$ signals on the data bus.
6) When 8259 received 2nd $\overline{INTA}$, it places the Low-order byte of the CALL address on the data bus. At 3rd $\overline{INTA}$, it places the higher byte on the data bus. CALL address is the vector address/location for the Interrupt.
7) During 3rd $\overline{INTA}$ pulse, the ISR bit is reset either automatically (Automatic End of Interrupt-AEOI) or by a command word must be issued at the end of the Service routine (End of Interrupt - EOI)
8) The program sequence is transferred to ME specified by the CALL Instr.



Interfacing of 8259 to 8085 MP

BLOCK Diagram of 8259 :-

It include eight blocks :- control logic, Read/Write logic, data bus Buffer, three Register (IRR, ISR and IMR), Priority Resolver and Cascade Buffer.

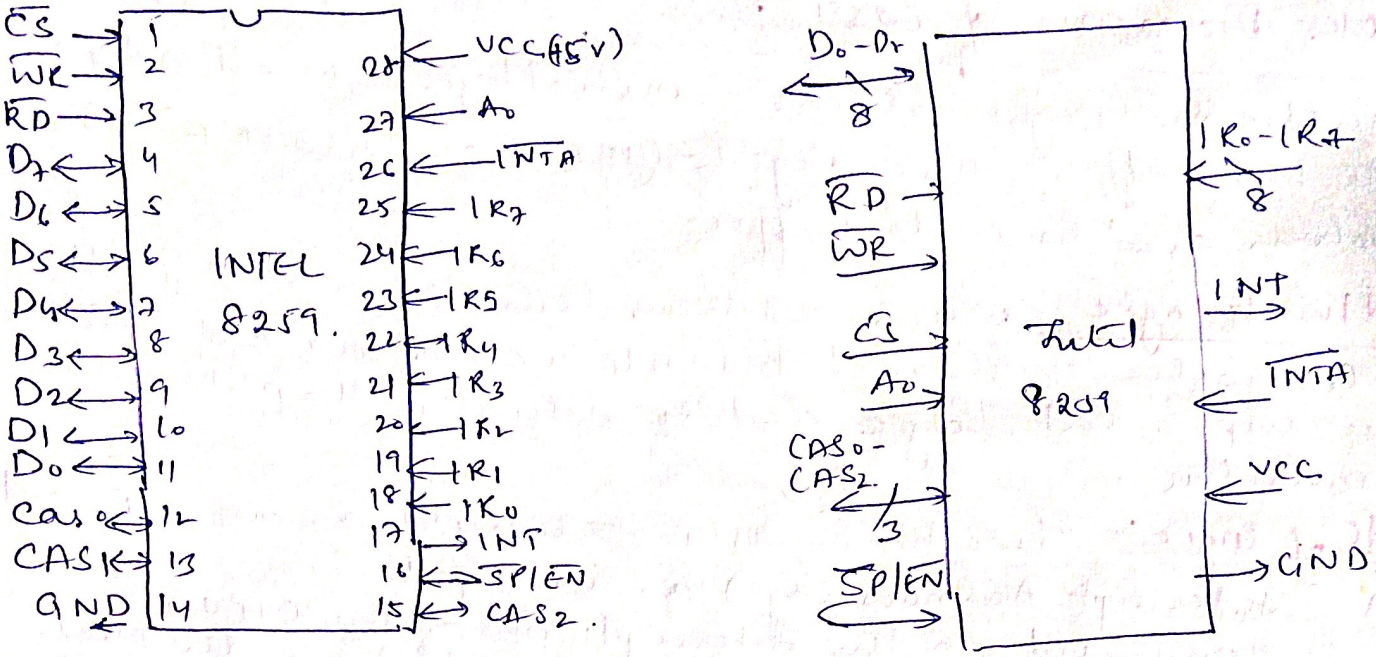
1) **Read/Write logic** - when address line A_0 is at logic 0, the controller is selected to write a cmd or read a status. The chip select logic and A_0 determine the port address of controller.

2) **control logic :-** Two pins :- INT (Interrupt) as an o/p, and $\overline{INTA}$ (Interrupt Acknowledge) as an input.
INT is connected to the interrupt pin of the CPU.
$\overline{INTA}$ is Interrupt Acknowledge signal from the MPU.

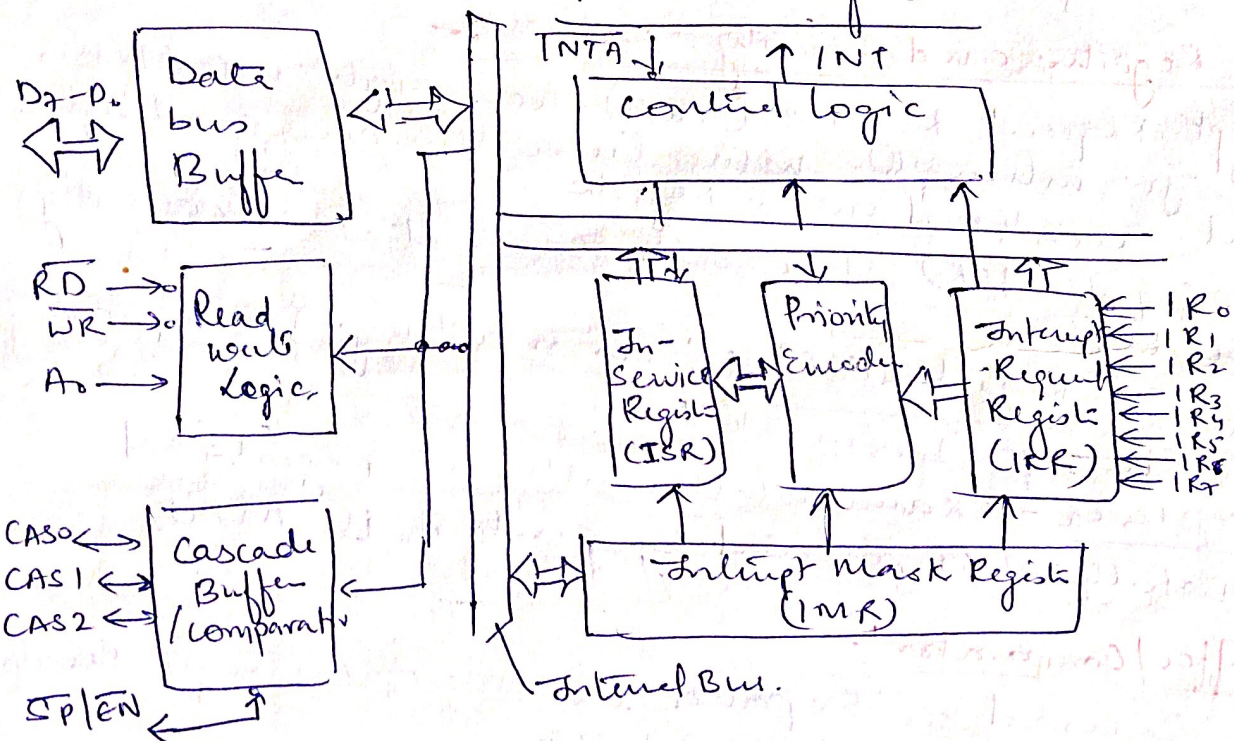
3) **Interrupt Register and Priority Resolver :-**
The Interrupt Request Register (IRR) has eight input lines ($IR_0 - IR_7$) for interrupts. when these lines are goes high, the request are stored in the Register.
- IN-Service Register (ISR) store all levels that are currently being executed.
- Interrupt Mask Register (IMR) stores masking bits of the Interrupt lines to be masked.
- Priority Resolver - examines these three register and determine whether INT should be sent to the MPU.

4) **Control Buffer/Comparator :-**
The block is used to expand the no. of Interrupt levels by cascading two or more 8259As.

$D_7 - D_0$ - Databus (Bi directional)	INT - Interrupt o/p
$\overline{RD}$ - Read I/P	$\overline{INTA}$ - Int Ack I/p
$\overline{WR}$ - Write I/P	$IR_0 - IR_7$ - Interrupt Request Inputs
A_0 - Command select address	
$\overline{CS}$ - Chip select	
$CAS_2 - CAS_0$ - Cascade lines	
$\overline{SP}/\overline{EN}$ - Slave Program/Enable Buffer	



Pin details of 8259.



Functional BLOCK Diagram of 8259

Priority Modes and other features

1) **fully Nested mode** - This general purpose mode in which all IRs (Int. Req) are arranged from Highest to lowest, with IR0 as the highest and IR7 as Lowest. In addition, IR can be assigned H Priority in this mode; the Priority sequence will then begin at the IR.
Ex:- IR4 has HP and IR3 has Lowest priority.

IR0	IR1	IR2	IR3	IR4	IR5	IR6	IR7
4	5	6	7	0	1	2	3
			↑	↑			
			LP	HP			

2) **Automatic Rotation mode** - A device, after being serviced, receives the LP. Assume IR2 has just serviced, it will receive the priority.

IR0	IR1	IR2	IR3	IR4	IR5	IR6	IR7
5	6	7	0	1	2	3	4

3) **Specific Rotation Mode** - Similar to Automatic mode, except user can select any IR for the LP, thus fixing all the priorities.

4) **End of Interrupt** - After the completion of an interrupt service, the corresponding ISR bit needs to be reset to update the information in the ISR. This called the (EOI) command.

1) **Non Specific EOI Cmd** - When this cmd sent to 8259A, it resets the (HP) ISR bit - High priority.

2) **Specific EOI cmd** - Following cmd specifies which ISR bit to reset.

3) **Automatic EOI** - No cmd is necessary. During the Third $\overline{INTA}$ the ISR bit is reset.

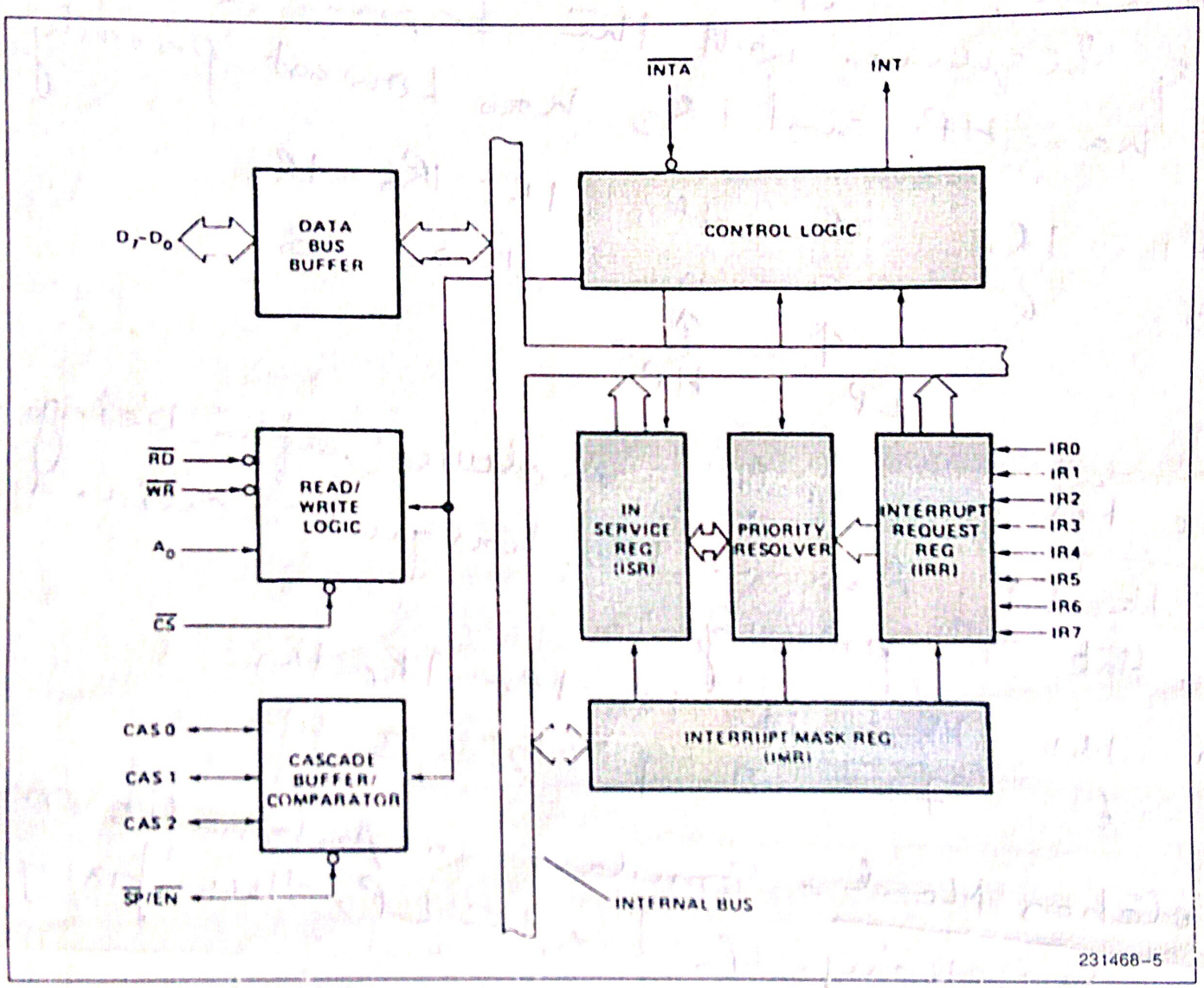


Figure 4a. 8259A Block Diagram

Interrupt

UNIT-3

Normal program execution is interrupted by some External Signals or by special Instruction called Interrupts. In response to an Interrupt, the MP stops executing its current program and calls a procedure called Interrupt service Routine (ISR). similar to subroutine.

S/W & H/W Interrupts

Interrupt caused by executing special Interrupt Instruction is called S/W Interrupts. There is interrupt are Restart Instruction (RST).

→ H/W – Interrupt caused by External Signals are called H/W Interrupt. 8085 MP processor has five pins for accepting external interrupt signal

There are TRAP, RST 7.5, RST 6.5, RST 5.5 and INTR.

highest priority

* TRAP – Non maskable Interrupt (can't be disabled).
* 4 (RST 7.5, 6.5, 5.5, INTR) – Maskable (can be disabled).
* INTR – Non vectored (require External H/w to get call location).

Lowest priority

Remaining all are vectored (have specific call location)

8085 Interrupt

- S/W Interrupt (RST 0, RST 1 ... RST 7)
- H/W Interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5 & INTR)
  - Vectored
    - TRAP (Non-Maskable)
    - RST 7.5, RST 6.5, RST 5.5 (Maskable)
  - Non vectored
    - INTR (Maskable)

Classification of 8085 Interrupts

⊗ S/W Interrupts

Call location — ?

Interrupt caused by executing RST instruction, inserted in the program are called S/W Interrupt.

8085 MP has 8 RST (Instructions).

- It similar to Call instruction and transfer the program execution to new location. But these location are predefined on page 00H of memory.

Diff: Call and RST Instruction is Call is 3 byte Instruction, RST — 1 byte Instruction. In case of RST is no need to specified call address, which is predefined.

RST instructions their codes in binary as well as in H Decimal and their call location are:-

RST Instruction

RST Instⁿ	Binary code								Hex Code	Call Location
	D7	D6	D5	D4	D3	D2	D1	D0		
RST 0	1	1	0	0	0	1	1	1	C7H	0000H
RST 1	1	1	0	0	1	1	1	1	CFH	0008H
RST 2	1	1	0	1	0	1	1	1	D7H	0010H
RST 3	1	1	0	1	1	1	1	1	DFH	0018H
RST 4	1	1	1	0	0	1	1	1	E7H	0020H
RST 5	1	1	1	0	1	1	1	1	EFH	0028H
RST 6	1	1	1	1	0	1	1	1	F7H	0030H
RST 7	1	1	1	1	1	1	1	1	FFH	0038H

H/W — TRAP (NMI) It can't be masked or disabled,
RST 7.5, 6.5, 5.5, (INTR (Maskable) enabled & disabled, required by programmer.

EI — Instⁿ is used to enable the Interrupt by setting the Internal Interrupt FF. After Execution of EI instruction, all maskable Interrupt (RST 7.5, 6.5, 5.5 and INTR) are enabled. TRAP is always enabled and not affected by EI Instruction.

RST Instructions –

Restart instruction are one byte call instruction called ~~location~~ for each restart instruction is predefined on page 0 (ROM). They transfer the program execution to the predefined memory location. These instructions also save the contents of the PC on the stack. They are software interrupts.

	called location
RST 0	0000
RST 1	0008
RST 2	0010
RST 3	0018
RST 4	0020
RST 5	0028
RST 6	0030
RST 7	0038

Interrupts – Normal program execution is interrupted by some external signals or by special instructions called interrupts. In response to an interrupt the microprocessors stops executing its urrent program and calls a procedure called interrupt service routine similar to subroutine.

B_7	B_6	B_5	B_4	B_3
x	x	x	0	1

8085 Interrupts

- Software Interrupts (RST0, RST1, ... RST7)
- Hardware Interrupts (TRAP, RST 7.5, RST 6.5, RST 5.5 and INTR)
  - Vectored
    - TRAP (Non Maskable)
    - RST 7.5, RST 6.5, RST 5.5 (Maskable)
  - Non Vectored
    - INTR (Maskable).
    - (External hard were required)

(classification of 8085 Interrupts).

Non Maskable — can not be disabled

Maskable — Can be enabled and disabled whenever required by the programmer.

(1) EI → All maskable interrupts (RST 7.5, RST 6.5, RST 5.5 and INTR) are enabled

TRAP — is always enabled and not affected by EI instruction.

(2) DI — (Disable Interrupt) — is used to disable RST 7.5, RST 6.5, RST 5.5 and INTR are disabled. TRAP is not affected by DI instruction.

RIM:- Read Interrupt Mask. This is a 1 byte Instruction can be used for following function.

1) Read Interrupt Mask - The Instruction load the Acc with 8bits indicating the current status of Interrupt masks.
2) To identify pending interrupt Bits D4, D5 and D6. identify pending Interrupt.
3) To receive serial data. Bit D7 is used to receive serial data.

7	6	5	4	3	2	1	0
SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5

- Interrupt mask: 1-masked, 0-unmasked
- Interrupt Enable flag: 1-enabled, 0-Disabled Interrupt
- Pending Interrupt: 1-pending, 0-Not pending Interrupt
- Serial Input data Bit, if any

Accumulator Bit Pattern for the RIM Instruction

Example Write a program segment to mask 6.5 and RST 5.5 Interrupt and enable RST 7.5 Interrupt

Solution - 8bit data to be loaded in Acc to enabling RST 7.5 and masking 6.5 and 5.5. The data to be loaded Acc is OBH

D7	D6	D5	D4	D3	D2	D1	D0	
x	x	x	0	1	0	1	1	= OBH

- D0: Unmask RST5.5
- D1: Mask RST6.5
- D2: Unmask RST 7.5
- D3: Mask set flag is enabled
- D4: RST7.5 Interrupt is Enabled
- D5, D6, D7: don't care

Program

```
EI      = Enable all Int of 8085
MVI A,0BH - Move 0B to Acc
SIM : Mask 6.5, 5.5 and Enable 7.5.
```

08/04/2014

RIM + SIM (Set Interrupt Mask) (Read interrupt mask)

* SIM:-

7	6	5	4	3	2	1	0
SOD	SDE	XXX	R7.5	MSE	M7.5	M6.5	M5.5

- RST 7.5 masked, RST 6.5 mask, RST 5.5 mask { 0 - Available, 1 - Masked }
- Ignored
- Mask set Enable { if 0, bits 0-2 ignored, if 1, mask is set }
- RESET RST 7.5 : if 1, RST 7.5 is reset off.
- if 1, bit 7 is O/P to serial O/P Data latch.
- Serial O/P data : ignored if bit 6 = 0.

ACCUMULATOR BIT PATTERN FOR THE SIM INTRUCTION

SIM :- Set Interrupt Mask. This 1byte instruction and can be used for 3 different function

1) One function is set mask for RST 7.5, RST 6.5 and RST 5.5 interrupt. Its read content of the Acc and enables or disables the interrupt according to the content of Acc.
2) Second function is reset RST 7.5. Bit D4 additional control for RST 7.5. D4 = 1, RST 7.5 is reset.
3) Third function to implement serial I/O. Bit D7 and D6 of the Acc are used for serial I/O and do not affect the interrupts. D6 = 1 enables the serial I/O.
   D7 = used to transmit (O/P) bits.

Pending Interrupt : Because there are several interrupt lines when one interrupt request is being served, other interrupt Request may occur and remain Pending. 8085 has additional Instruction called RIM (Read Interrupt Mask) to serve the Pending Interrupt.