Before going into more details of CMOS, let us briefly understand what are logic families. Integrated Circuit or chip is a device that has number of circuits integrated as one entity. Since IC is a way simplify the complexity, there are many types of circuit configurations that are used in the production if integrated circuits.

All these circuit configuration approaches are known as Logic Families. The idea behind logic families is that different logic functions of a circuit when fabricated as an IC that are put together using a single approach will have same electrical characteristics.

Some of these characteristics are power dissipation, power supply, speed, noise etc.

As most of the ICs are manufactured using either Bipolar Devices or MOS Device, the logic families are also divided into two families: The Bipolar families and the MOS families.

**Bipolar Logic Families**

The following is a list of the Bipolar Logic Families.

- Diode Logic (DL)
- Resistor Transistor Logic (RTL)
- Diode Transistor Logic (DTL)
- Transistor Transistor Logic (TTL)
- Emitter Coupled Logic (ECL)
- Integrated Injection Logic ($I^2L$)

**MOS Logic Families**

The following is a list of the MOS Logic Families.

- PMOS Family (uses p-Channel MOSFET)
- NMOS Family (uses n-Channel MOSFET)
- CMOS Family (uses both p-Channel MOSFET and n-Channel MOSFET)

There is another logic family called Bi-CMOS Family which uses both Bipolar devices as well as MOS devices.

**PMOS and NMOS Technologies**

Before the extensive use of CMOS Technology for implementing logic gates and in fabrication of ICs, PMOS and NMOS logic were widely used. In fact, the Intel 4004 and the initial version of Intel 8008 are fabricated using PMOS technology.

PMOS was later replaced by the NMOS technology, which is one of the widely used IC Fabrication technologies (before CMOS). Initially, even CMOS was slower and expensive than NMOS.

NMOS became the "standard process" for integrated circuits. The main advantages of NMOS technology are simple physical process, high functional density, good speed (initially faster than CMOS) and easier to manufacture.

The main drawbacks of NMOS technology are its electrical asymmetry and static power dissipation. All these drawbacks are minimized by the CMOS Technology.

**CMOS Technology**

The CMOS Technology uses both NMOS and PMOS to realize various logic functions. Both the N-channel MOSFET and the P-channel MOSFET are design in such a way that they have matching characteristics (during ON and OFF state).

The main advantage of CMOS technology over Bipolar or the previous popular NMOS technologies is its extremely low power consumption in static conditions as they draw power only during switching operation.

This allows integrating much larger number of logic gates on the VLSI IC when compared to Bipolar or NMOS technologies.

Today, CMOS technology is the dominant IC fabrication technology in VLSI industry and is used for making high end microprocessors, microcontroller, memory modules, sensors and Application Specific Integrated Circuits (ASICs).

The combination of NMOS and PMOS devices in a CMOS logic makes it easier to design different logic functions. With the improvements in CMOS IC fabrication technologies, the size of the transistor can be scaled down in size.

| Course Outcomes | |
|---|---|
| CO-1 | Understanding various model, non-ideal, switching and inverter characteristics of MOS |
| CO-2 | Understand and analyze delay, design rule and circuit layout of CMOS |
| CO-3 | Analyze various parameter(power dissipation, Transistor sizing , gate delay) of combinational CMOS logic family |
| CO-4 | Analyze and Evaluate dynamic CMOS circuits. |
| CO-5 | Design Custom/ASIC design using FPGA kit through VHDL code. |

## Introduction

Integrated electronic circuits which are based on complementary metal-oxide-semiconductor **(CMOS)** technologies are firmly established in modern electronics. CMOS provides the important characteristics needed for high-density logic designs. Moreover, with recent developments in the field of BiCMOS, it is anticipated that we have a technology which will provide a transition to the next century. CMOS, which is short for Complimentary Metal-Oxide Semiconductor, is a predominant technology for manufacturing integrated circuits. This dominance of CMOS Technology in the fabrication of Integrated Circuits or ICs will continue for decades to come.

Generally, the CMOS Technology is associated with VLSI or Very Large-Scale Integrated Circuit, where a few millions or even billions of transistors (MOSFETs to be specific) are integrated into a single chip or die.

The reasons for the dominant use of CMOS Technology in the fabrication of VLSI chips are reliability, low power consumption, considerably low cost and most importantly scalability.

You might have heard of the famous Moore's Law described by Gordan Moore, according to whom, the number of devices on a chip will double every 18 to 24 months. Even though Gordan Moore did not imply it to CMOS, the Moore's Law been successfully fulfilled due to the CMOS technology.

Today, we are dealing with channel lengths as small as 7nm (at the time of publishing this tutorial), all because of the scaling ability in CMOS.

### Logic Families

## 7EC5-13: CMOS Design (program elective-3)

**Credit: 3**
**3L+0T+0P**

**Max. Marks: 150(IA:30, ETE:120)**
**End Term Exam: 3 Hours**

| SN | Contents | Hours |
|---|---|---|
| 1 | Introduction: Objective, scope and outcome of the course. | 01 |
| 2 | Review of MOS transistor models, Non-ideal behavior of the MOS Transistor, Transistor as a switch, Inverter characteristics | 08 |
| 3 | Integrated Circuit Layout: Design Rules, Parasitic, Delay: RC Delay model, linear delay model, logical path efforts, Power, interconnect and Robustness in CMOS circuit layout | 07 |
| 4 | Combinational Circuit Design: CMOS logic families including static, dynamic and dual rail logic.<br>NAND Gate, NOR gate, XOR gate, Compound Gates, 2 input CMOS Multiplexer, Memory latches and registers, Transmission Gate, estimation of Gate delays, Power dissipation and Transistor sizing. Basic physical design of simple Gates and Layout issues. Layout issues for CMOS inverter, Layout for NAND, NOR and Complex Logic gates, | 10 |
| 5 | Dynamic CMOS circuits- Clocked CMOS ($C^2MOS$) logic, DOMINO logic, NORA logic, NP(ZIPPER) logic, PE (pre-charge and Evaluation) Logic. Basic Memory circuits, SRAM and DRAM. | 08 |
| 6 | Physical Design- Introduction to ECAD tools for first and back end design of VLSI circuits. Custom /ASIC design, Design using FPGA and VHDL. VHDL Code for simple Logic gates, flip-flops, shift registers. | 06 |
| | **Total** | 40 |

| **Text/Reference Books:** | |
|---|---|
| 1. | N.H.E. Weste and D.M. Harris, CMOS VLSI design: A Circuits and Systems Perspective, 4thEdition, Pearson Education India, 2011. |
| 2. | Sung-Mo-Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits Analysis &Design, McGraw Hill |
| 3. | C.Mead and L. Conway, Introduction to VLSI Systems, Addison Wesley, 1979. |
| 4. | J. Rabaey, Digital Integrated Circuits: A Design Perspective, Prentice Hall India, 1997. |
| 5. | P. Douglas, VHDL: programming by example, McGraw Hill, 2013. |
| 6. | L. Glaser and D. Dobberpuhl, The Design and Analysis of VLSI Circuits, Addison Wesley, 1985. |