Co-3 : Analyze various parameter(power dissipation, Transistor sizing , gate delay) of combinational CMOS logic family

## Learning Outcomes (LO)

Students will able to learn

LO-1 : Combinational Logic Circuit Design(NAND , NOR ,Compound, Memory and Latches).

LO-2 : Transistor sizing, Gate delay, Power dissipation.

LO-3 Physical design rules of CMOS .

LO-4 : Layout issues for CMOS.

Lo-5 : Layout of NAND, NOR Gates.

## NAND GATE :-

Nand gate analysis consist of n parallel driver transistors. Current $I_D$ in this circuit is than current $I_D$ in the circuit is supplied by driver transistor which are turned 'on'

The combined pull-down current can.

$$I_D = \sum_{K(On)} I_{D,K} = \begin{cases} \sum_{K(On)} \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right)_K \left[2(V_{GS,K} - V_{TO}) V_{out} - V_{out}^2\right] & \text{if } V_{out} < V_{GS} - V_{TO} \rightarrow \text{linear} \\ \sum \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right)_K (V_{GS,K} - V_{TO})^2 & \text{if } V_{out} \geq V_{GS} - V_{TO} \rightarrow \text{saturation} \end{cases}$$

Assuming that the input voltage of all driver transistors are identical

$$V_{GS,K} = V_{GS} \text{ for } K = 1, 2 \ldots n$$

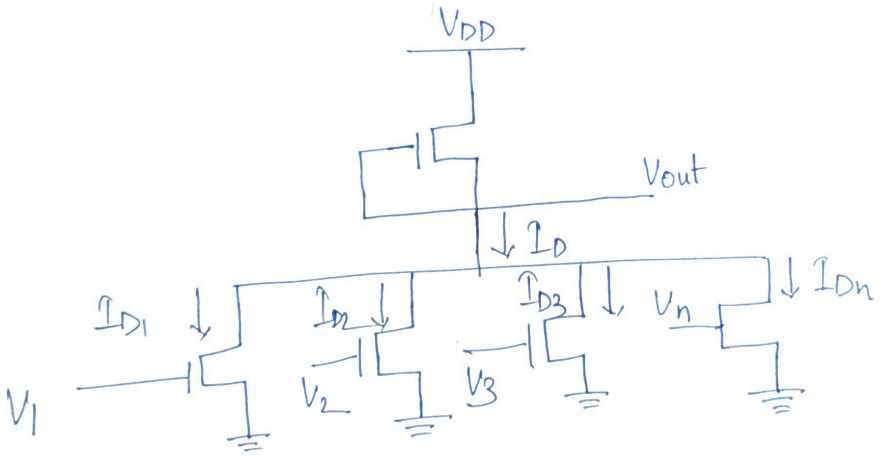



Fig: Generalized n-input NOR Gate.

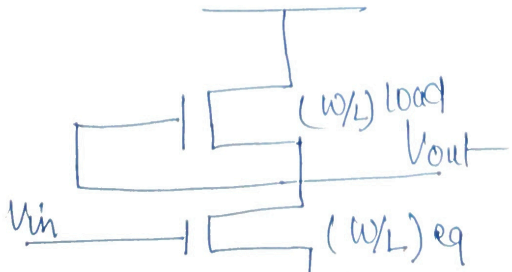



Fig: Equivalent inverter circuit Corresponding to n-input NOR gate

Pull down current expression can be written as

$$I_D = \begin{cases} \frac{\mu_n C_{ox}}{2} \left( \sum_{k(on)} (W/L)_k \right) [(V_{GS} - V_{T0})(V_{out} - V_{out}^2)] & \text{linear} \\ \frac{\mu_n C_{ox}}{2} \left( \sum_{k(on)} (W/L)_k \right) (V_{GS} - V_{T0})^2 & \text{saturation} \end{cases}$$

An multiple-input NOR gate can be reduced to an equivalent inverter for static analysis

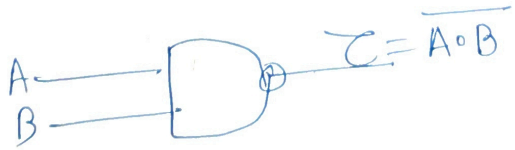
The $(W/L)$ ratio of driver transistor

$$\left(\frac{W}{L}\right)_{eq} = \sum_{(k\,on)} \left(\frac{W}{L}\right)_k$$

## Two-Input NAND Gate :-

| $V_A$ | $V_B$ | $V_{out}$ |
|---|---|---|
| Low | Low | high |
| Low | high | high |
| high | Low | high |
| high | high | low |

Truth-table of 2 Input NAND Gate



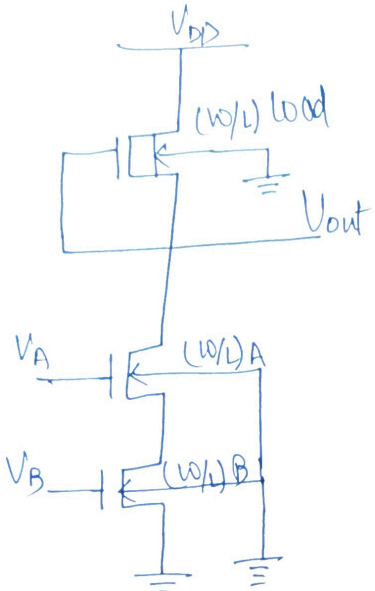



Fig: A two-input depletion-load NAND gate.

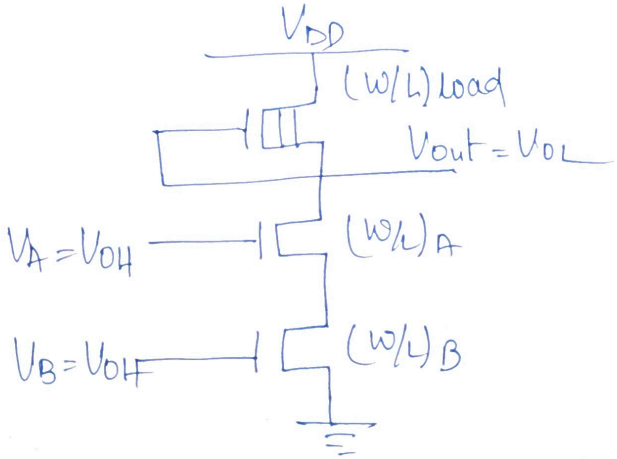



Fig: 2 input NAND gate with both side high inputs.

Generalized NAND Gate Expression:

$$I_D = \frac{\mu_n C_{ox}}{2} \left( \frac{1}{\sum_{K(On)} \left[ \frac{1}{(W/L)_K} \right]} \right) \begin{cases} 2[V_{in} - V_{TO}] V_{out} - V_{out}^2 & \text{Linear} \\ (V_{in} - V_{TO})^2 & \text{Saturation} \end{cases}$$

W/L ratio of driver circuit

$$\left(\frac{W}{L}\right)_{eq} = \frac{1}{\sum_{K(ON)} \frac{1}{\left(\frac{W}{L}\right)_K}}$$

If series connected transistor are identical $(W/L)_1 = (W/L)_2 = \cdots$

$(W/L)$ than $(W/L)$ becomes.

$$\left(\frac{W}{L}\right)_{eq} = \frac{1}{n}\left(\frac{W}{L}\right)$$

## CMOS (Two Input NOR Gate) NOR)

In two input NOR Gate the two input Voltages $V_A$ & $V_B$ are applied to the gates of one nMOS & one pMOS transistor.

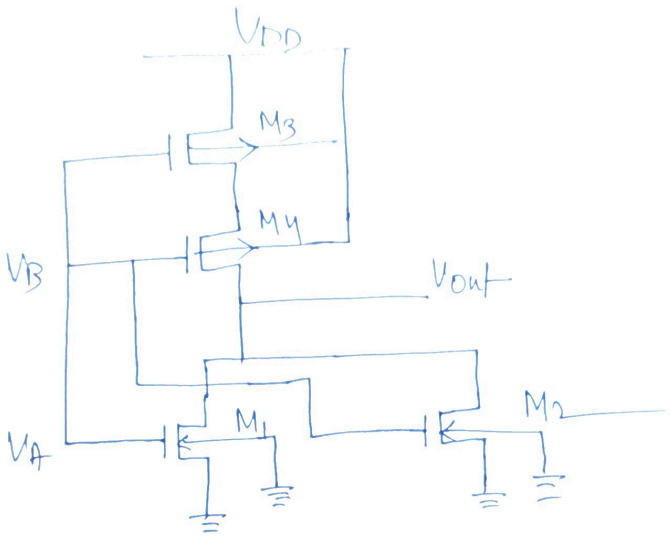



Fig: CMOS NOR gate.

The Output Voltage of CMOS NOR2 gate will attain a logic - low Voltage of $V_{OL}=0$ & high Voltage $V_{OH}=V_{DD}$.

$V_A = V_B$ & $(W/L)_{n,A} = (W/L)_{n,B}$.

The Output Voltage is equal to Input Voltage

$$V_A = V_B = V_{out} = V_{th}.$$

two parallel nMOS transistor are saturated at this point because $V_{GS} = V_{DS}$

$$\boxed{I_D = k_n (V_{TH} - V_{T,n})^2}$$

First eqn. for Switching threshold $V_{th}$

$$V_{th} = V_{T,n} + \sqrt{\frac{I_D}{K_n}}$$

NMOS operates in linear region while other transistor NM4 in saturation

$V_{in} = V_{out}$

$$I_{D3} = \frac{K_P}{2}\left[2(V_{DD} - V_{th} - |V_{T,P}|)V_{SD3} - V_{SD3}^2\right]$$

$$I_{D4} = \frac{K_P}{2}\left(V_{DD} - V_{th} - |V_{T,P}| - V_{SD3}\right)^2$$

the drain current of both PMOS transistors are identical. $I_{D3} = I_{D4} = I_D$

$$\boxed{V_{DD} - V_{th} - |V_{T,P}| = 2\sqrt{I_D/K_P}}$$

this yeild second eqn of switching threshold voltage $V_{th}$

$$V_{th(NOR2)} = \frac{V_{T,n} + \frac{1}{2}\sqrt{\frac{K_P}{K_n}}(V_{DD} - |V_{T,P}|)}{1 + \frac{1}{2}\sqrt{\frac{K_P}{K_n}}}$$

Now Compare this expression with switching expression of CMOS.

$$V_{th(INR)} = \frac{V_{T,n} + \sqrt{\frac{K_P}{K_n}}(V_{DD} - V_{T,P})}{1 + \sqrt{\frac{K_P}{K_n}}}$$

If $K_P = K_n$ & $V_{T,n} = |V_{T,P}|$ then

$$\boxed{V_{th(NOR2)} = \frac{V_{DD} + V_{T,n}}{3}}$$

which is not equal to $V_{DD}/2$

The switching threshold voltage of NOR 2 gate inverters are obtained by using equivalent inverter approach.

$$V_{th(NOR2)} = \frac{V_{T,n} + \sqrt{\frac{K_P}{2K_n}}\left(V_{DD} - |V_{T,P}|\right)}{1 + \sqrt{\frac{K_P}{2K_n}}}$$

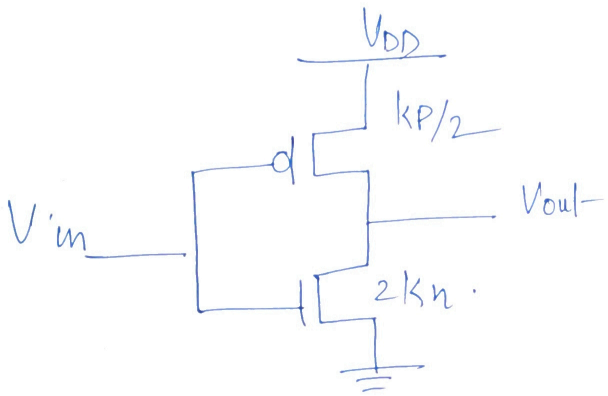



Fig: CMOS NOR 2 inverter equivalent ckt.

## 2 Input CMOS Multiplexer :-

Mux is a data selector that selects one of several analog or digital input signals & forward the selected input into a single output line.

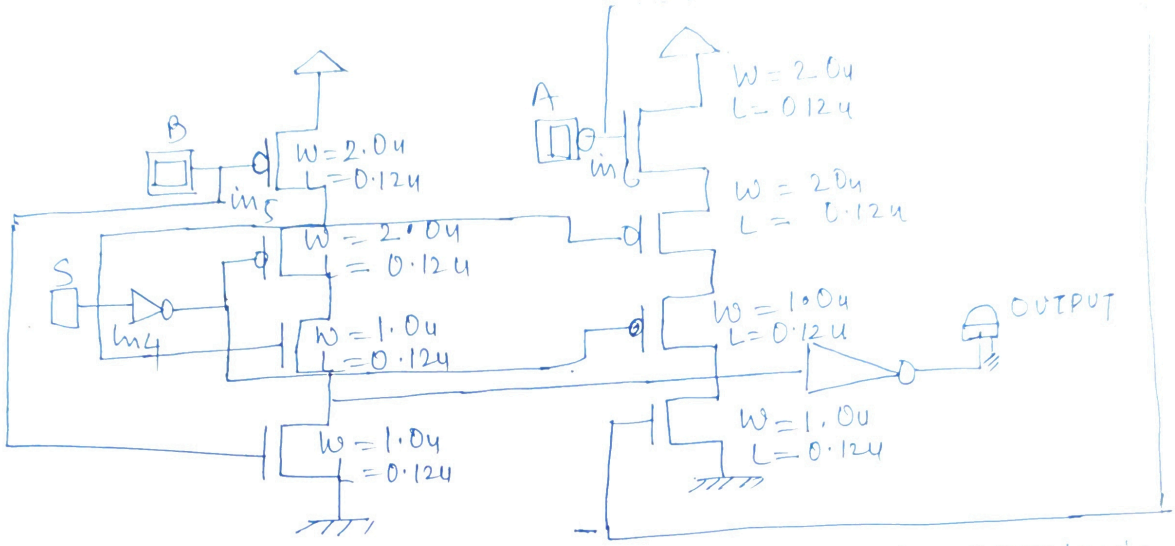



Fig: Schematic of 2:1 MUX using CMOS logic

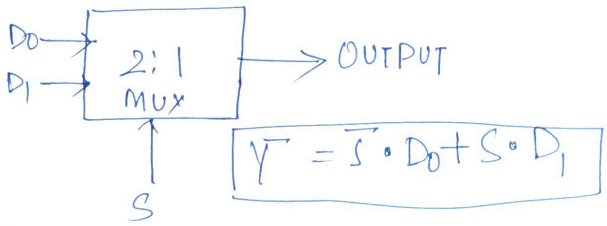



Fig: Block digram of 2:1 MUX

| SELECT LINE | INPUT | | OUTPUT |
|---|---|---|---|
| S̄/S | D1 | D0 | Y |
| 1/0 | X | 0 | 0 |
| 1/0 | X | 1 | 1 |
| 0/1 | 0 | X | 0 |
| 0/1 | 1 | X | 1 |

Truth-Table of 2 Input CMOS Multiplexer.

## MEMORY LATCHES & REGISTERS:

NAND & NOR gate are normally used in designing of SR, JK & D latch.

i) S-R latch

ii) Using NOR gate

### SR- latch


Fig: Block diagram of SR-latch

| S | R | $Q_{n+1}$ |
|---|---|---|
| 0 | 0 | $Q_n$ |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | Indeterminate |

Table: Truth Table of SR latch

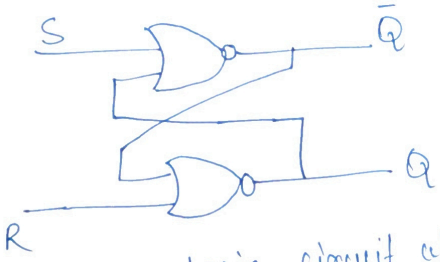



Fig: logic circuit of SR latch

we have $\bar{Q} = \overline{S+Q}$ & $Q = \overline{R+\bar{Q}}$

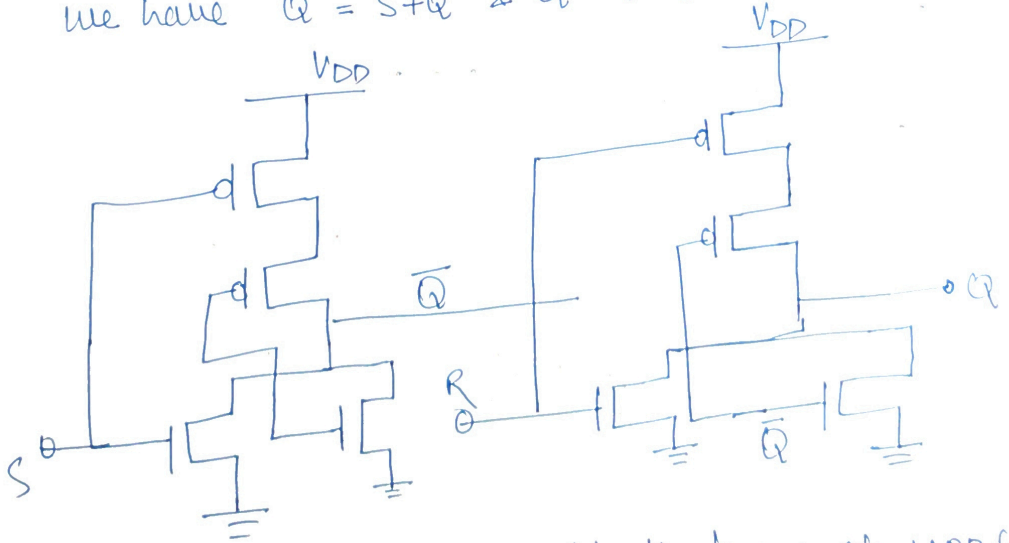



Fig: CMOS SR latch circuit based on NOR Gate

Using NAND Gate

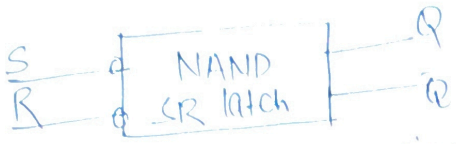



Fig: SR Latch using NAND Gate

| S | R | $Q_{n+1}$ |
|---|---|---|
| 0 | 0 | Indeterminate |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | $Q_n$ |

Table: Truth Table

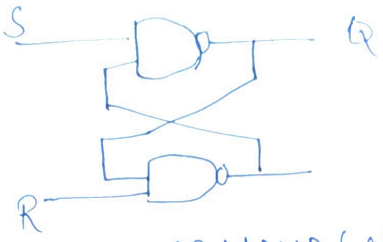



Fig: NAND Gate based SR logic circuit

We have $Q = \overline{S \cdot \bar{Q}}$ and $\bar{Q} = \overline{R \cdot Q}$

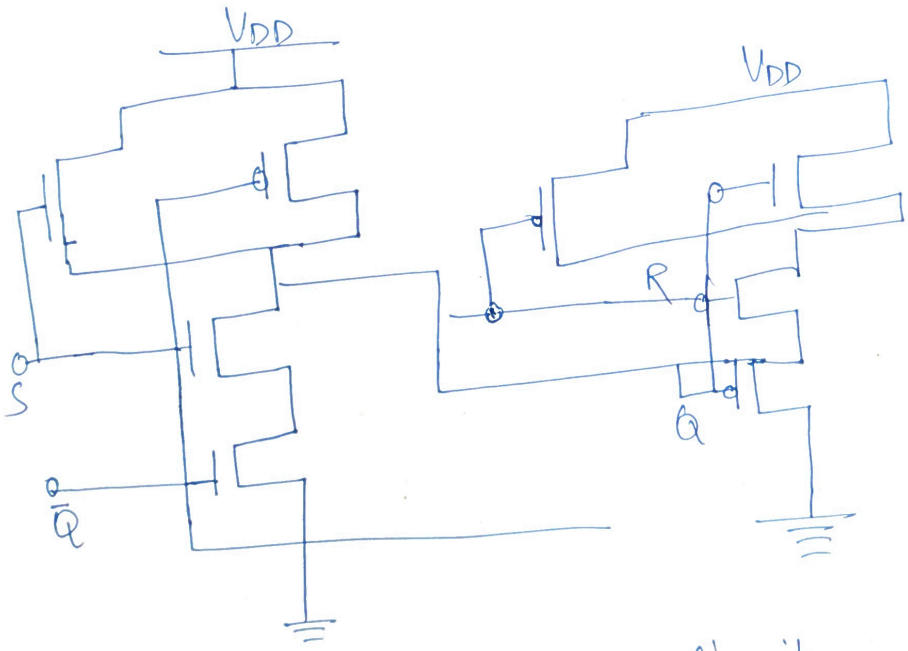



Fig: CMOS SR latch circuit

## D-LATCH :-


fig: Block diagram

| CLK | D | $Q_{n+1}$ |
|---|---|---|
| 0 | x | $Q_n$ |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

fig: Truth Table

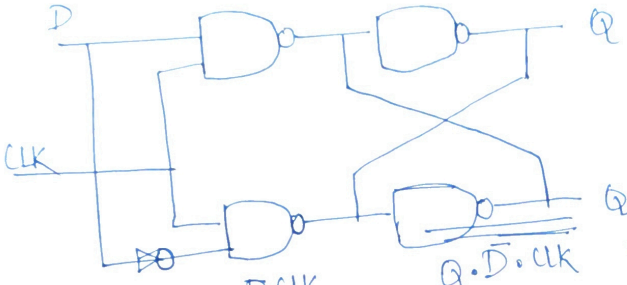



fig: D latch Logic circuit

Table: Truth Table

| J | K | $Q_{n+1}$ |
|---|---|---|
| 0 | 0 | $Q_n$ |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | $\bar{Q}_n$ |

## JK LATCH :-

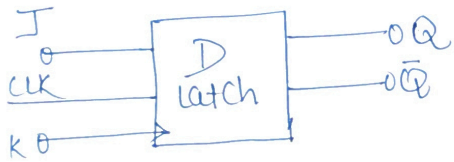



fig: Block digram of D latch

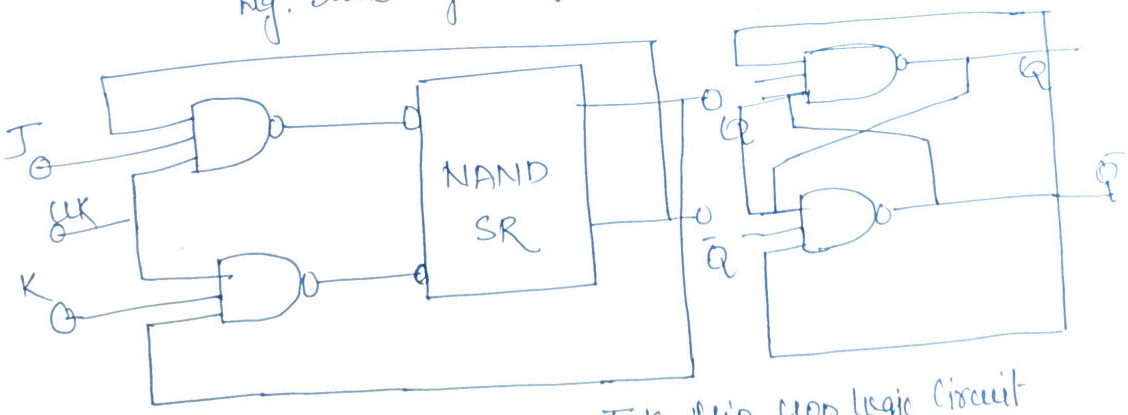



fig : JK flip-flop logic circuit

## Registers :-

Generally Registers are used for temporary storage of data or binary information within the digital system.

⇒ Registers are also used for shifting the binary information stored in it.

⇒

Register
- Buffer Registers
- Serial in Serial Out (SISO)
- Serial in parallel Out (SIPO)
- Parallel in Serial Out (PISO)
- Parallel in parallel Out (PIPO)

## BUFFER REGISTERS

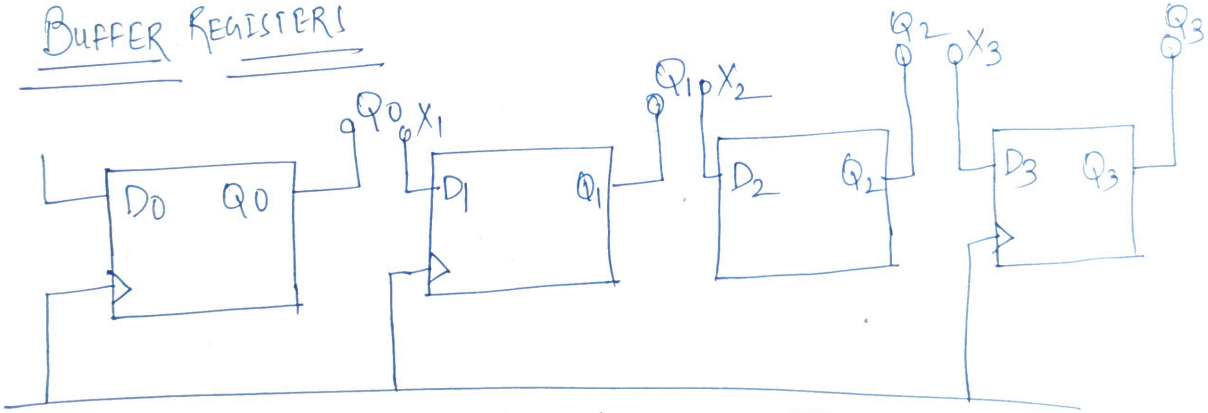



Fig: 4 bit buffer register

SISO

## T- LATCH

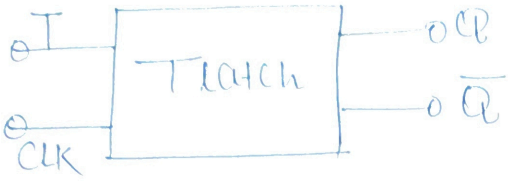



Fig: Block diagram of T latch.

| T | $Q_{n+1}$ |
|---|---|
| 0 | $Q_n$ |
| 1 | $\bar{Q}_n$ |

Table: Truth Table

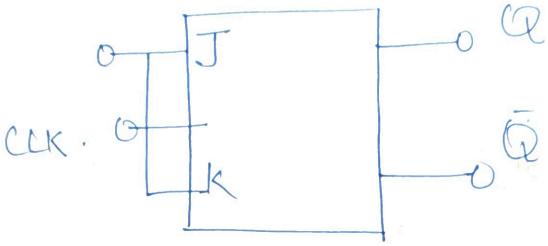



Fig:

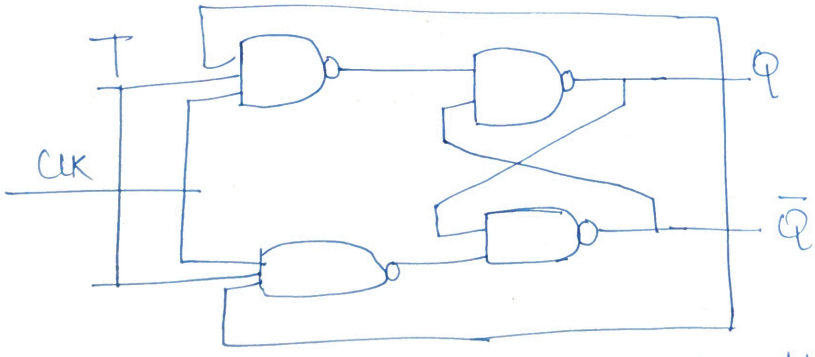



Fig: logic diagram of T latch using NAND gate.

## TRANSISTOR SIZING :

⇒ In the designing of CMOS circuit we have to decide W/L ratio for all the devices. These ratio usually are selected to provide the gate with current driving capability in both direction which is equal to that of the basic Inverter.

⇒ In device sizing we find the input combination that result in the lowest output current and then choose sizes that we will make this current equal to that of the basic Inverter.

⇒ We need to find W/L ratio is base of the resistance is inversely proportional to W/L.
If numes of MOSFETs having ratio of $(W/L)_1, (W/L)_2, -$ $(W/L)_n$ then

$$r_{ds} = \frac{1}{K(W/L)(V_{GS}-V_t)}$$

$$r_{ds} = \frac{\text{constant}}{(W/L)}$$

$$\text{constant} = \frac{1}{K(V_{GS}-V_t)}$$

If MOSFET are connected in Serial than

$$R_{eq} = r_{ds1} + r_{ds2} + \cdots r_{dsn}$$

$$\frac{\text{constant}}{(W/L)_{eq}} = \frac{\text{constant}}{(W/L)_1} + \frac{\text{constant}}{(W/L)_2} + \cdots \frac{\text{constant}}{(W/L)_n}$$

$$\frac{1}{(W/L)_{eq}} = \frac{1}{(W/L)_1} + \frac{1}{(W/L)_2} + \cdots \frac{1}{(W/L)_n}$$

⇒ If MOSFET are connected in parallel then for $(W/L)_{eq}$.

$$\frac{1}{R_{eq}} = \frac{1}{r_{ds_1}} + \frac{1}{r_{ds_2}} + \cdots + \frac{1}{r_{ds_n}}$$

$$\frac{1}{\left[\frac{\text{constant}}{(W/L)_{eq}}\right]} = \frac{1}{\left[\frac{\text{constant}}{(W/L)_1}\right]} + \frac{1}{\left[\frac{\text{constant}}{(W/L)_2}\right]} + \cdots + \frac{1}{\left[\frac{\text{constant}}{(W/L)_n}\right]}$$

$$\Rightarrow \left(\frac{W}{L}\right)_{eq} = \left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)_2 + \cdots \left(\frac{W}{L}\right)_n$$

For consideration of $(W/L)_{eq}$, when all transistors are ON in both cases (series or ||).

⇒ When the transistors are connected in series, and all the transistors are ON.

⇒ When the transistors are connected in parallel, and any one is only ON.