Co-1 : Understanding various model, non-ideal, switching and inverter characteristics of MOS.

Learning Outcomes (LO)

LO-1 Students will able to Learn

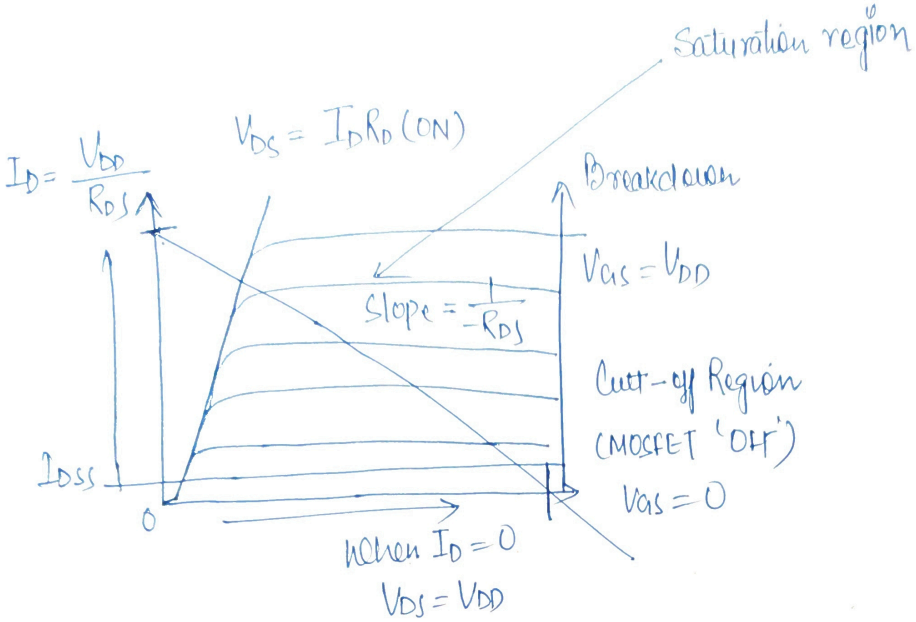
LO-2 MOS Transistor MODELS.

LO-3 Non- ideal behavior of MOS.

LO-4 Transistor as a switch

LO-5 Inverter Characteristics

MOSFET characteristics Curve :-



1) Cut-Off Region :-

The Operating condition of the transistor are zero input gate voltage (V_{IN}) zero drain current I_D and Output voltage. $V_{DS} = V_{DD}$.

Therefore for an enhancement type MOSFET the conducting channel is closed & device is switched 'OFF'.

* The input & Gate are grounded (0V).
* Gate - Source voltage less than threshold voltage.

$V_{GS} < V_{TH}$

* MOSFET is "OFF" (cut-off region)
* No Drain current flows ($I_D = 0$ Amps)
* MOSFET Operates as an "Open Switch".

Thus we can define cut-off region or 'OFF' mode when using an e-MOSFET as a switch as being.

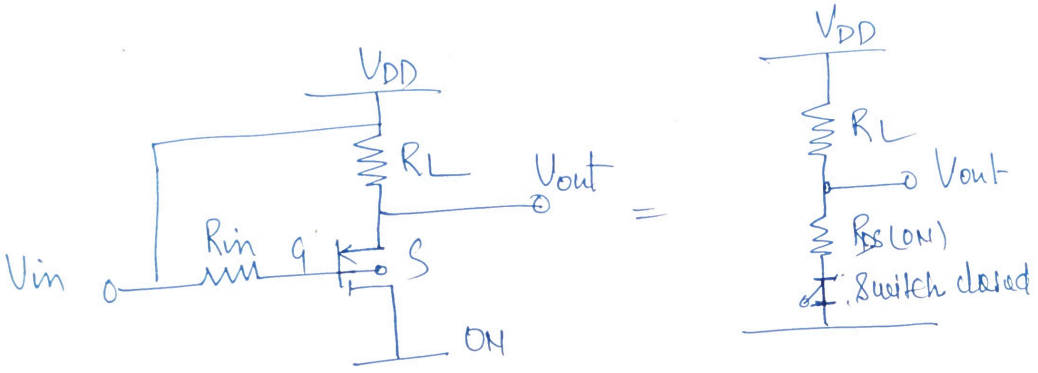
gate voltage, $V_{GS} < V_{TH}$ then $I_D = 0$

For a p-channel enhancement MOSFET, the gate potential must be more positive with respect to the Source.

SATURATION REGION :-

In saturation or linear region the transistor will be biased. So that the maximum amount of gate voltage is applied to the device which results in the channel resistance $R_{DS(ON)}$ being as small as max^{m} drain current flowing through MOSFET switch.

Therefore enhancement type MOSFET conducting channel is open and device is switched 'ON'



* The input & Gate are connected to V_{DD}.
* Gate - Source voltage is much greater than threshold voltage
  $V_{GS} > V_{TH}$
* MOSFET is "ON" (Saturation region)
* Max Drain Current

$$\boxed{I_D = V_{DD}/R_L}$$

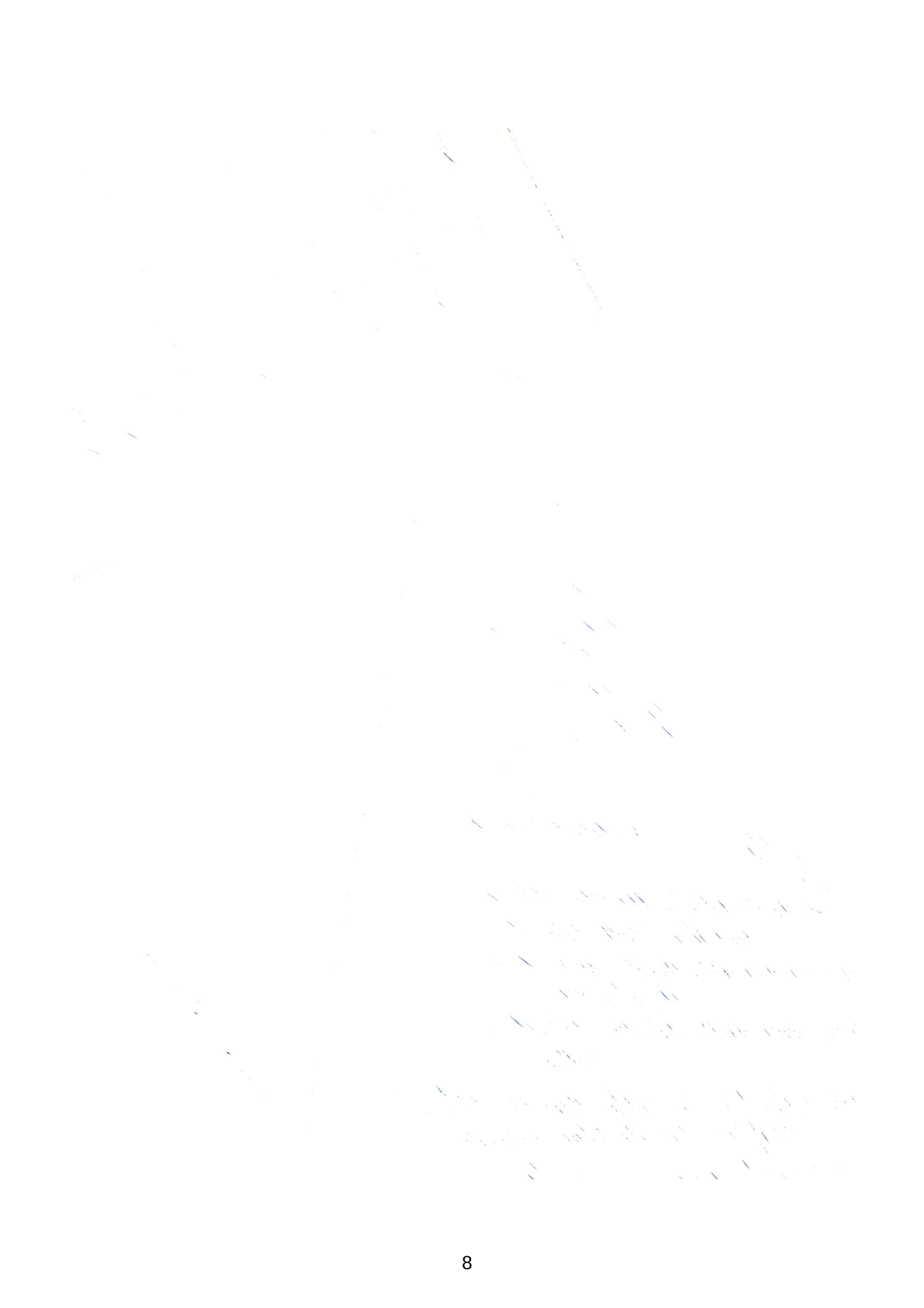
min^{m} channel resistance

$R_{DS(ON)} < 0.1\Omega$

MOSFET operates as low resistance "closed switch"

Saturation region or 'ON' mode when using an e-MOSFET as a switch gate - Source voltage $V_{GS} > V_{TH}$

then $I_D =$ Max^{m}



CMOS INVERTER :-

⇒ CMOS inverter consist of an enhancement type nMOS transistor and an enhancement type PMOS transistor.

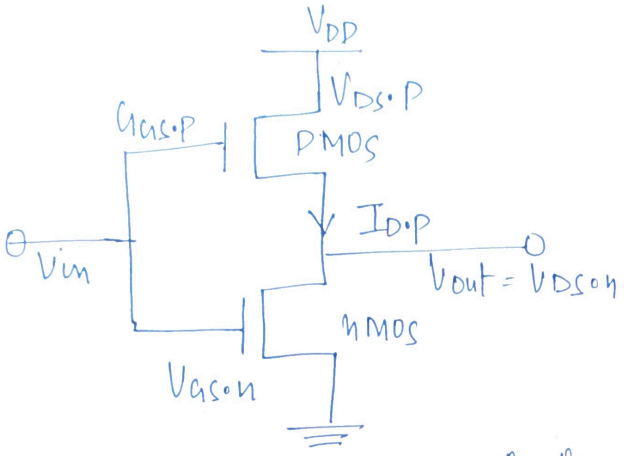


Fig: CMOS inverter circuit

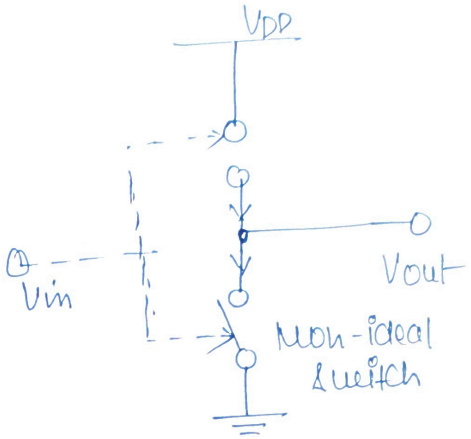


Fig: Non-ideal CMOS inverter switches.

The main advantage of CMOS inverter are

⇒ Low power dissipation

⇒ Voltage transfer curve show full swing of output from 0 to VDD.

⇒ Sharp transition between states which increase noise margin.

— NMOS transistor Operates in $V_{in} > V_{TO,n}$ and if the following condition is satisfied.

$V_{DS.n} \geq V_{gs.n} - V_{TO.n} \iff V_{out} \geq V_{in} - V_{TO,n}$

— Thus PMOS transistor Operates in saturation if Vin

$V_{in} < (V_{DD} + V_{TO,P})$

$V_{DS.P} \leq V_{gs.n} - V_{TO.P} \iff V_{out} \leq V_{in} - V_{TO.P}$

Table:

Region	V_{in}	V_{out}	nMOS	PMOS
A	$V_{TO,n}$	V_{OH}	Cut-off	Linear
B	V_{IL}	high $\approx V_{OH}$	Saturation	Linear
C	V_{th}	V_{th}	Saturation	Saturation
D	V_{IH}	lower V_{OL}	Linear	Saturation
E	$> (V_{DD} - \lvert V_{TO,p} \rvert)$	V_{OL}	Linear	Cut-off

⇒ In region A where $V_{in} < V_{TO,n}$ the nMOS transistor is cutoff and the voltage is equal to $V_{OH} = V_{DD}$ as the input voltage is increased beyond $V_{TO,n}$ (into region B), the n-MOS transistor starts conducting in saturation mode & Output voltage begins to decrease.

⇒ Also note that Critical voltage V_{IL} which corresponds to $\frac{dV_{out}}{dV_{in}} = -1$ is located into region B.

⇒ As the Output voltage further decreases, the PMOS transistor enters at the boundary at region C.

⇒ When Output voltage falls below $(V_{in} - V_{TO,n})$ the nMOS transistor starts to operate in linear mode.

⇒ This corresponds to region D, where the critical point V_{IH} with $\left| \frac{dV_{out}}{dV_{in}} \right| = -1$ is also located.

Finally in region I with input voltage $V_{in} > (V_{DD} + V_{TO,P})$ the PMOS transistor is cut-off and the output voltage is $V_{OL} = 0$.

Calculation of V_{OH} :

When $V_{in} < V_{TO,n}$ the nMOS transistor is cutoff & PMOS in linear region

$I_{Dn} = 0$, So $I_{DP} = 0$

$$\boxed{I_{Dn} = I_{DP} = 0}$$

So drain source voltage of PMOS is zero & $V_{out} = V_{in}$ PMOS in linear region.

$$I_{DP} = \frac{K_P}{2}\left(2\left[V_{GS,P} - V_{TO,P}\right]V_{DS\cdot P} - V_{DS\cdot P}^2\right] = 0 \quad \text{---(1)}$$

$$\frac{K_P}{2}\left[2(V_{GS,P} - V_{TO,P})\right]\left[-V_{DD} - V_{OH}\right] - \left[-V_{DD} - V_{OH}\right]^2 \quad \text{---(2)}$$

The valid solution is

$$\boxed{V_{OH} = V_{DD}}$$

Calculation of V_{OL}

When the input voltage exceeds $V_{DD} + V_{TO\cdot P}$ the PMOS transistor is cutoff & nMOS transistor is ON.

Since $V_{in} - V_{TO,n} > V_{out}$ $(V_{DD} + V_{TO\cdot P} - V_{TO} > V_{OL})$

nMOS transistor is in linear region PMOS in Cut-off

So drain current is zero

$$\boxed{I_{DP} = I_{Dn} = 0}$$

So we have

$$\frac{K_n}{2}\left[2(V_{GS,n} - V_{TO,n})V_{out} - V_{out}^2\right] = 0$$

Substituting $V_{out} = V_{OL}$ in above eqn

$[V_{OL} = 0]$

Calculation of V_{th} :-

The Inverter threshold voltage V_{th} is defined as the voltage for which $V_{in} = V_{out}$

When the input & Output are same then PMOS & nMOS transistor are in saturation.

So equating the current

$$\frac{K_n}{2}(V_{GS,n} - V_{TO,n})^2 = \frac{K_p}{2}(V_{GS,p} - V_{th} - V_{TO,p})^2$$

Substituting for $V_{GS,n}$ & $V_{GS,p}$ from eq^{n} becomes

$$\frac{K_n}{2}(V_{in} - V_{TO,n})^2 = \frac{K_p}{2}(V_{in} - V_{DD} - V_{TO,p})^2$$

$V_{in} = V_{TH}$ eq^{n} becomes quadratic becomes

$$V_{th} = \frac{V_{TO,n} + \sqrt{\frac{K_p}{K_n}}(V_{DD} - V_{TO,p})}{\left(1 + \sqrt{\frac{K_p}{K_n}}\right)}$$

Calculation of V_{IL} :-

=> V_{IL} is the smaller of two input voltage for which slope of voltage transfer curve is -1.

=> When the input is low the nMOS transistor is in saturation and the PMOS transistor is in linear region.

$$\frac{K_n}{2}(V_{GS,n} - V_{TO,n})^2 = \frac{K_p}{2}\left[2(V_{GS,p} - V_{TO,p})(V_{GS,p} - V_{DS,p}) - V_{DS,p}^2\right] \quad \text{— (I)}$$

for CMOS Inverter we have

$V_{GS,n} = V_{in}$

$V_{DS,n} = V_{out}$

$$V_{GS,p} = -(V_{DD} - V_{in}) \quad \text{— (II)}$$

$$V_{DS,p} = -(V_{DD} - V_{out}) \quad \text{— (III)}$$

Substituting the value of (II) & (III) in eqn (I) we have.

$$\frac{K_n}{2}(V_{in} - V_{TO,n})^2 = \frac{K_p}{2}\left[2(V_{in} - V_{DD} - V_{TO,p})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2\right] \quad \text{— (IV)}$$

Differentiating eqn (IV) we have.

$$K_n(V_{in} - V_{TO,n}) = K_p\left[(V_{in} - V_{DD} - V_{TO,p})\frac{dV_{out}}{dV_{in}} + (V_{out} - V_{DD}) - \left[V_{out} - V_{DD} - \frac{dV_{out}}{dV_{in}}\right]\right]$$

$V_{in} = V_{IL}$ & $\frac{dV_{out}}{dV_{in}} = -1$ So we have.

$$K_n(V_{IL} - V_{TO,n}) = K_p(2V_{out} - V_{IL} + V_{TO,p} - V_{DD})$$

rearranging the terms obtained in V_{IL}

$$V_{IL} = \frac{V_{IL} - 2V_{out} + V_{TO,p} - V_{DD} - \frac{K_n}{K_p}V_{TO,n}}{1 + \frac{K_n}{K_p}}$$

V_{IL} is obtained numerically by solving eqn.

MOSFET as a Switch :

Enhancement mode N-channel MOSFET is being used as a 'switch' 'ON' & 'OFF'.

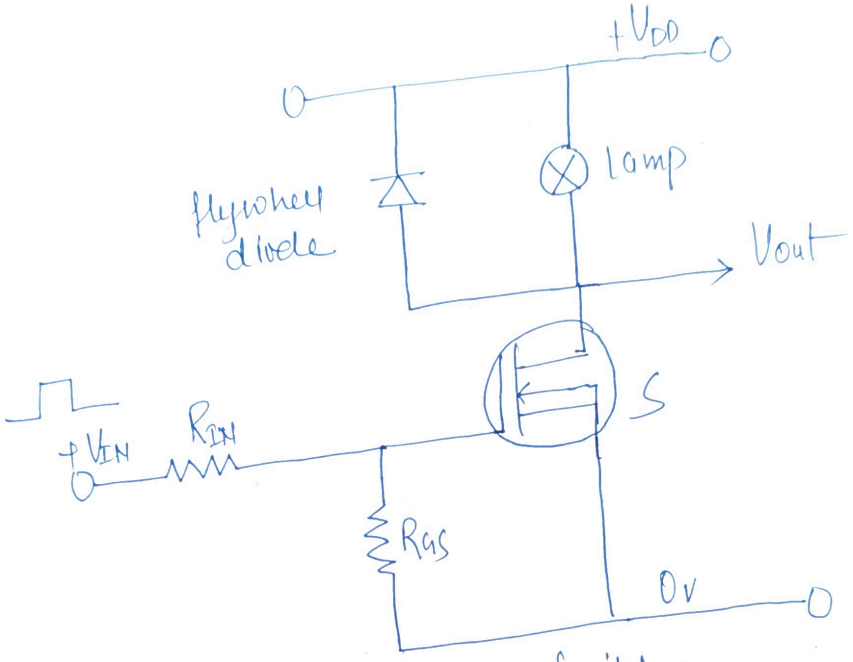


Fig : MOSFET as a Switch.

⇒ The gate input voltage VGS is taken to an appropriate positive voltage level to turn the device and therefore the lamp load either 'ON (VGS = +ve) or at Zero voltage level that turns the device 'OFF' (VGS = 0V).

⇒ If the resistive load of a lamp was replaced by an inductive load such as coil, Solenoid or relay a 'flywheel diode' would be required in parallel with the load to protect the MOSFET from any self generated back emf.

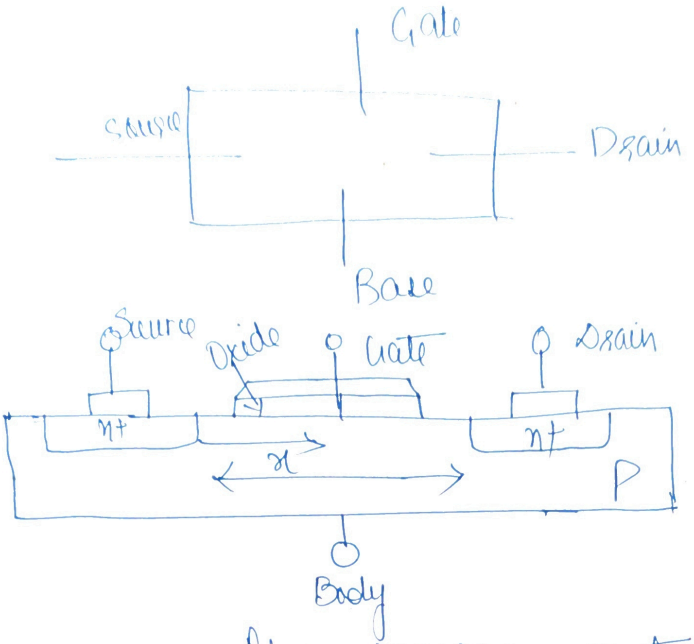


Fig: MOSFET with terminals

IDEAL MOSFET SWITCH CHARACTERTICS :-

When MOSFET is supposed to function as a switch.

⇒ In the ON condition there has to be current limitation that it carries.

⇒ In the OFF condition, blocking voltage level should not hold any kind of limitations.

⇒ When the device function in ON state, the voltage drop value should be null.

⇒ The resistance in OFF state should be infinite

⇒ There should no restrictions on the speed of Operation.