JAIPUR ENGINEERING COLLEGE AND RESERCH CENTRE

Academic Year: 2020-2021 (ODD Semester)

ELECTRONICS AND COMMUNICATION DEPARTMENT

Assignment No:2

CO: **Understand and analyze delay, design rule and circuit layout of CMOS.**

Short Answer Type

Q-1) What is delay in CMOS?

Q-2) Explain the purpose of Lambda design rule.

Long Answer Type

Q-1) What are layout design rules. Explain lambda design rule with their advantages.

Q-2) What is delay in CMOS What happens to delay if you increase load capacitance?

Q-3) What is the typical low to high propagation delay?

Q-4) Distinguish between linear and propagation delay

Q-5) Explicate power Delay in CMOS.

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ELECTRONICS AND COMMUNICATION DEPARTMENT

Assignment No:3

CO: Analyze various parameter (power dissipation, Transistor sizing, gate delay) of combinational CMOS logic family

Short Answer Type

Q-1) Why leakage power dissipation has become an important issue in deep submicron technology in deep submicron technology?

Q-2) What is the average propagation delay time?

Q-3)How can you combine sizing and supply voltage scaling to realize low power circuits?

Long Answer Type

Q-1) Explicate Transistor sizing.

Q-2) What are the key characteristics of MOS dynamic circuits?

Q-3) Design a 3-input CMOS NAND gate (PUN/PDN) with fan-out of 3. Total output load of the NAND gate is equal to 15fF and $\mu n/\mu p = 2.5$. For 0.35µm process technology tox = 7.6*10-9m, $\varepsilon ox = 35*10\text{-}12F/m$. Compare the above design with that of a 3-input NOR (PUN/PDN) gate. State any benefits of one implementation over the other. For the sake of simplicity assume all capacitance is lumped and gate capacitance neglecting diffusion and wiring capacitance.

Q-4) Consider a circuit as follows: An inverter driving a transmission gate driving a capacitive load (all three in series). Design the transmission gate and inverter when the lumped capacitive load is equal 30fF. In addition, assume that there is wiring capacitance of 15fF as well. Design the inverter for a fan-out of 2 for high performance. Assume $\mu n = 0.04m2$ /Vs, $\mu p = 0.016m2$ /Vs, $Vtn = |Vtp| = 0.7$, Vdd = 3.3V. Size the TG to ensure the equivalent RC delay to be equal to 18ps.

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ELECTRONICS AND COMMUNICATION DEPARTMENT

Assignment No:4

SUBJECT: CMOS DESGIN (7EC5-13)

CO: Analyze and Evaluate dynamic CMOS circuits.

Short Answer Type

Q-1 What makes dynamic CMOS circuits faster than static CMOS circuits?

Q-2) What are the key characteristics of MOS dynamic circuits? What are the key characteristics of MOS dynamic circuits?

Q-3) Compare the sources of power dissipation between static CMOS and dynamic CMOS circuits?

Long Answer Type

Q-1) Compare the area, in terms of the number of transistors, for the three different implementations of a full adder using (i) static CMOS, (ii) domino CMOS, and (iii) complementary pass transistor logic (CPL).

Q-2) Explicate the basic operation of a 2 Q2. Explain the basic operation of a 2-phase dynamic phase dynamic circuit?

Q-3) How clock skew problem is overcome in NORA CMOS circuits?

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Academic Year: 2020-2021 (ODD Semester)

ELECTRONICS AND COMMUNICATION DEPARTMENT

Assignment No:4

SUBJECT: CMOS DESGIN (7EC5-13)

CO: Design Custom/ASIC design using FPGA kit through VHDL code.

Short Answer Type

Q-1) What is routing congestion. How to solve it?

Q-2) Explicate partial floor planning.

Q-3) How threshold Voltage effect timing in MOS.

Q-4) What is 9 track, 12 track standard cell.

Q-5) What is signal integrity. Ho it effects time?

Long Answer Type

Q-1) Explicate is the full custom ASIC design.

Q-2) In what ways do thermal parameters affect the interconnect-centric routing during VLSI Physical Design?

Q-3) What is the role of physical design engineer in CMOS VLSI?