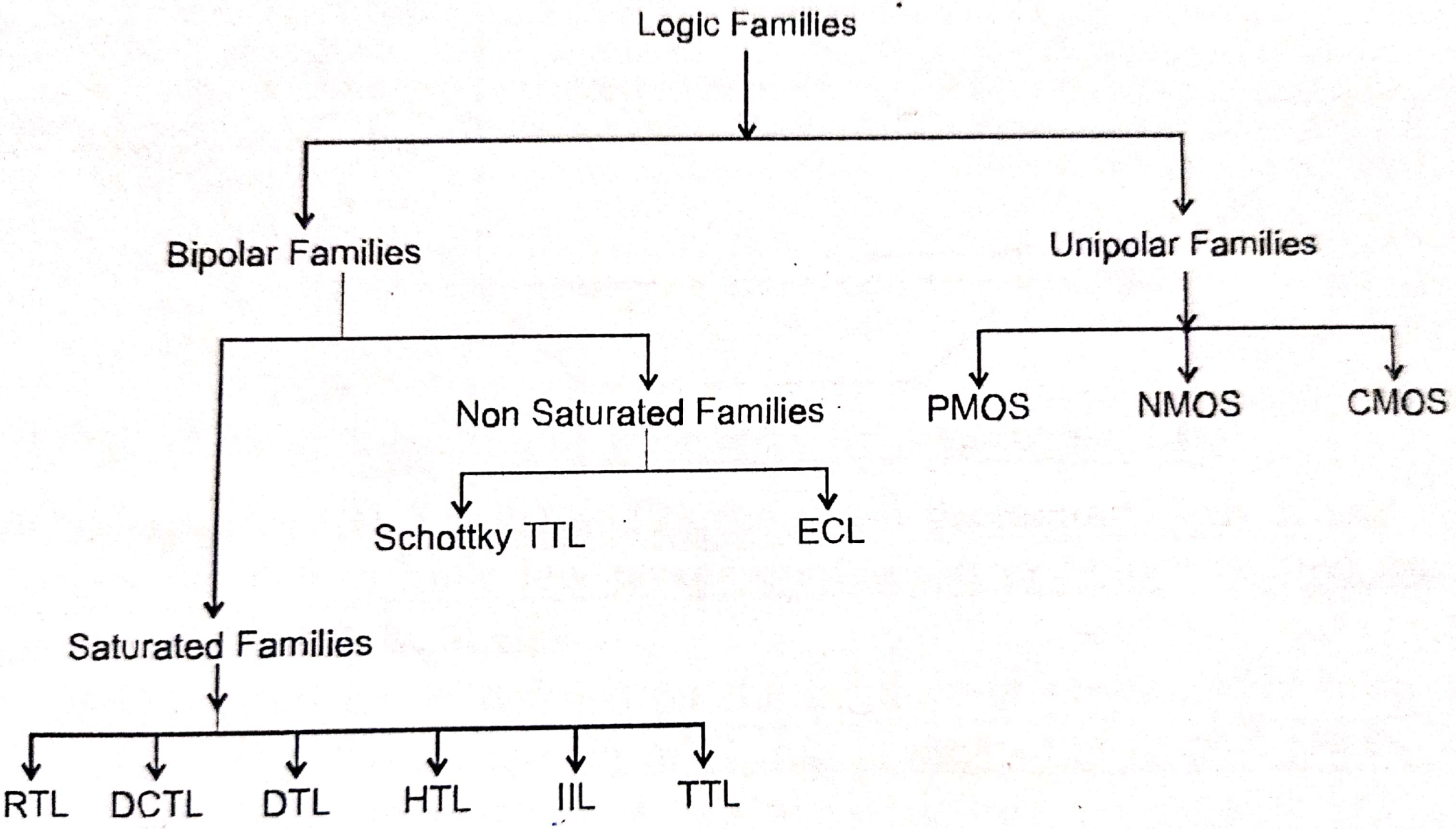


Fig. 10.28 Clasification of Locig Families.

10.2.2 Characteristics of Digital ICs and families

Emergence of various logic families and integration techniques have resulted in widespread use of digital ICs. It is thus necessary to study different performance parameters and characteristics of logic families. They adequately reflects their relative advantages and disadvantages and may serve as a basis to choose a particular family for the application. Infact our study and analysis of different families will be around these parameters only.

- **Propagation Delay** is the maximum time taken by output to change its state in response to input. The propagation delay determines the speed of operation of a gate. In general switching speed is measured when 50% duty cycle time square wave is applied at a input and a square wave is generated at output, as shown in Figure 10.28(*a*). The times are measured from 50% of voltage levels. The time t_{PHL} is delay when output goes LOW from HIGH and t_{PLH} is the time delay taken by output to go HIGH from LOW state. The propagation delay t_p is average of the two times and measured in *n* sec.

It is the average transition delay time for a signal to propagate from input to output when the binary signals change in value.

Active Time

$$t_p = \frac{t_{PHL} + t_{PLH}}{2} = \text{Propagation Delay } (n \text{ sec})$$

nanoseconds

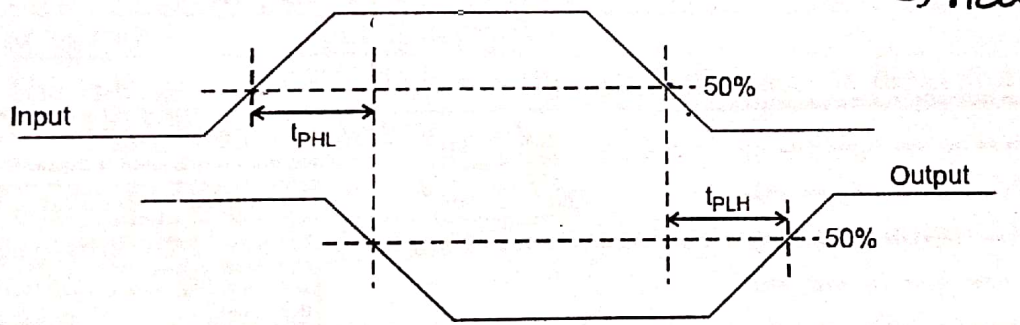


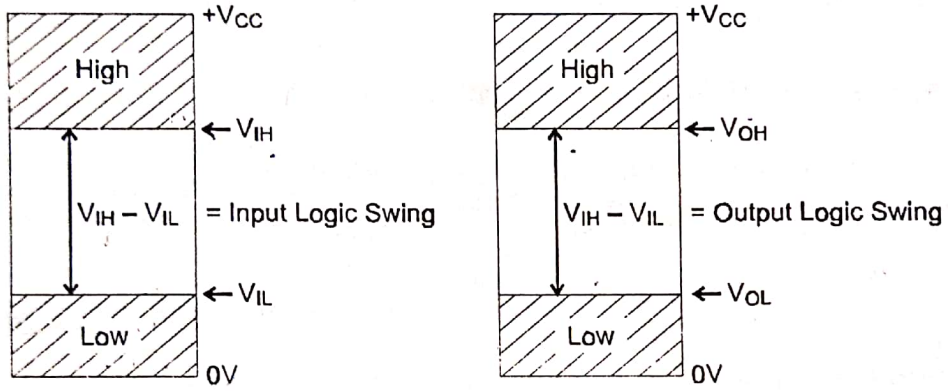
Fig. 10.28(*a*) Input-output waveforms for propagation delay

- **Power Dissipation (P_D)** is defined as the power dissipated in an IC and measured in mW. It is desired to have low power dissipation to reduce cooling, but it may increase the propagation delays.
- **Speed power product** is defined as the product of propagation delay (in nano seconds) and power dissipation (in mW) and is measured in pico joules. It is also referred as the figure of merit of a digital IC.

figure of merit = Propagation delay × Power Dissipation
= $t_p \times P_D$ = n sec × mW
= pJ

- **Fan In** is defined as the number inputs that a logic gate can have
- **Fan Out** is defined as number of similar gates that a logic gate can drive. High fan out is desirable.
- **Input and Output Voltages** various input and output voltage levels are shown in Fig. 10.29.

(i) **High Level Input Voltage (V_{IH})** is defined as the minimum input voltage recognized as logic 1.



(a) Input Voltage Profile (b) Output Voltage Profile

Fig. 10.29 Illustration of Voltage Profiles

Low Level Input Voltage (V_{IL}) is defined as maximum value of input voltage recognized as logic 0.

High Level Output Voltage (V_{OH}) is defined as the minimum value of output voltage when output is logic 1.

Low Level Output Voltage (V_{OL}) is defined as the maximum voltage that appears at output when output is logic 0.

The voltage separation between the two logic states is defined as the *logic swing*.

Input logic swing = $V_{IH} - V_{IL}$

Output Logic swing = $V_{OH} - V_{OL}$

- **Input and Output Currents** The important input and output currents are shown in Fig. 10.30.

HIGH LEVEL INPUT CURRENT (I_{IH}) is defined as the minimum current that must be supplied to a gate corresponding to logic 1 input.

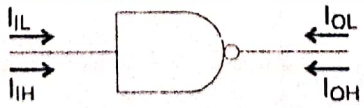


Fig. 10.30 Illustration of currents in a gate

Low Level Input Current (I_{IL}) is defined as the minimum current that must be supplied to the gate corresponding to logic 0 input.

High Level Output Current (I_{OH}) is defined as the maximum amount of current that a gate can sink when output is logic 1.

Low Level Output Current (I_{OL}) is defined as the maximum amount of current that a gate can sink when output is logic 0.

Why we have shown the output currents as sink current will be clear when discussing the circuits of various families.

- **Supply Currents** it is important to consider the current drawn in **low** and **high** state.

High State Supply Current ($I_{CC}(1)$) is the current drawn from supply when output of gate is logic 1.

Low State Supply Current ($I_{CC}(O)$) is the current drawn from supply when output of gate is logic O.

We can calculate average power dissipation by calculating the dissipation in two states.

The Low state power dissipation $P(O) = V_{CC}.I_{CC}(0)$

The High state power dissipation $P(1) = V_{CC}.\ I_{CC}(1)$

The average power dissipation $Pavg = \dfrac{P(1) + P(0)}{2}$

This is how we will calculate the power dissipation of various families in next sections.

- **Noise Margin** Unwanted electric signals, called noise, can appear when connecting the logic devices. These noise signals can cause the voltage levels to rise or reduce from intended value. This may cause circuit malfunction. For example if noise causes an input voltage to reduce below the V_{IH}, then input is not recognized as logic 1 and thus the circuit malfunctions. The ability of a circuit to tolerate the effect of noise is called as **noise immunity.** The amount by which a circuit can tolerate the effect of noise is called **noise margin.** The noise margins are illustrated in Fig. 10.31. Margins shown in the figure are called **dc noise margin,** they are

$\Delta 1 = V_{OH} - V_{IH}$ = High state noise margin

$\Delta O = V_{IL} - V_{OL}$ = Low state noise margin

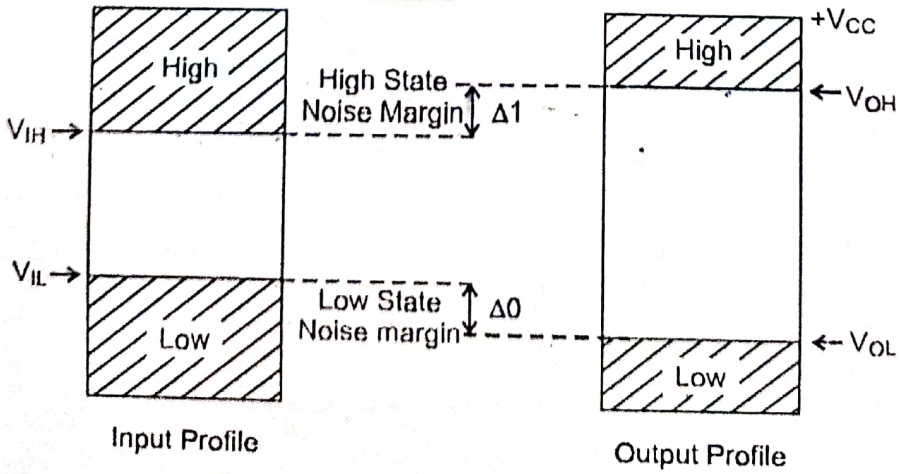


Fig. 10.31 Illustration of Noise Margins.

10.3.3 Direct Coupled Transistor Logic (DCTL)

The Basic DCTL gate is a NOR gate shown in Fig. 10.39. Comparing the Fig. 10.39 with Fig. 10.38(a) reveals the fact that DCTL is a RTL gate with no base resistor. Infact output of driver is directly connected to load and hence the name DCTL. Naturally in this case LOW output voltage is $V_{CE_{sat}} = 0.2$ V and the HIGH output voltage is $V_{BE_{sat}} = 0.8$ V. But the output logic swing is very small (0.8 – 0.2 = 0.6 V). Thus the noise margin is poor.

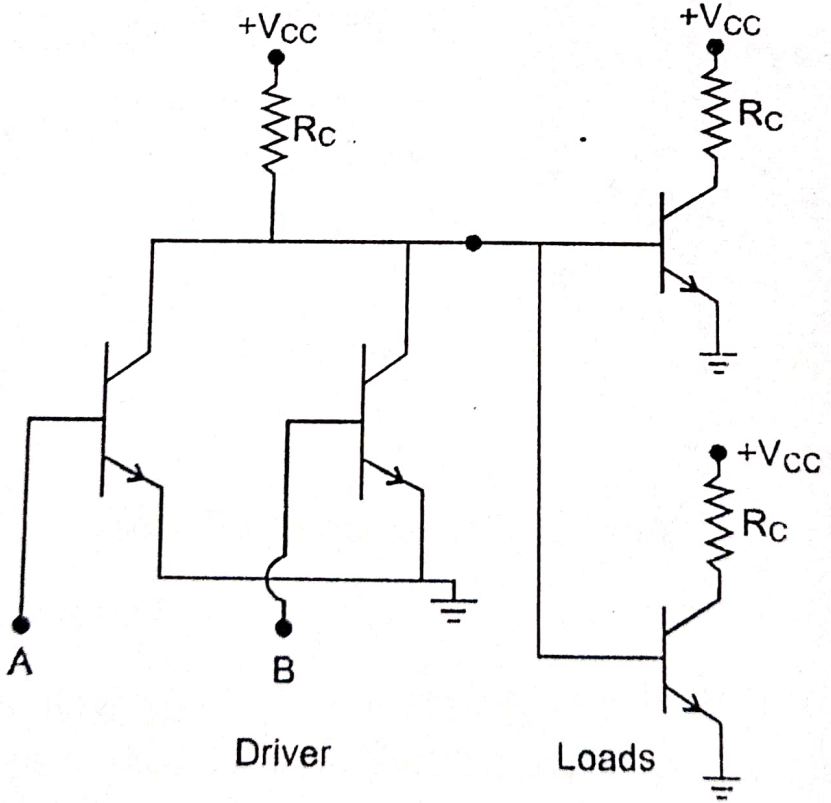


Fig. 10.39 Basic DCTL NOR Gate.

The DCTL gates are simpler than RTL but suffer from ...

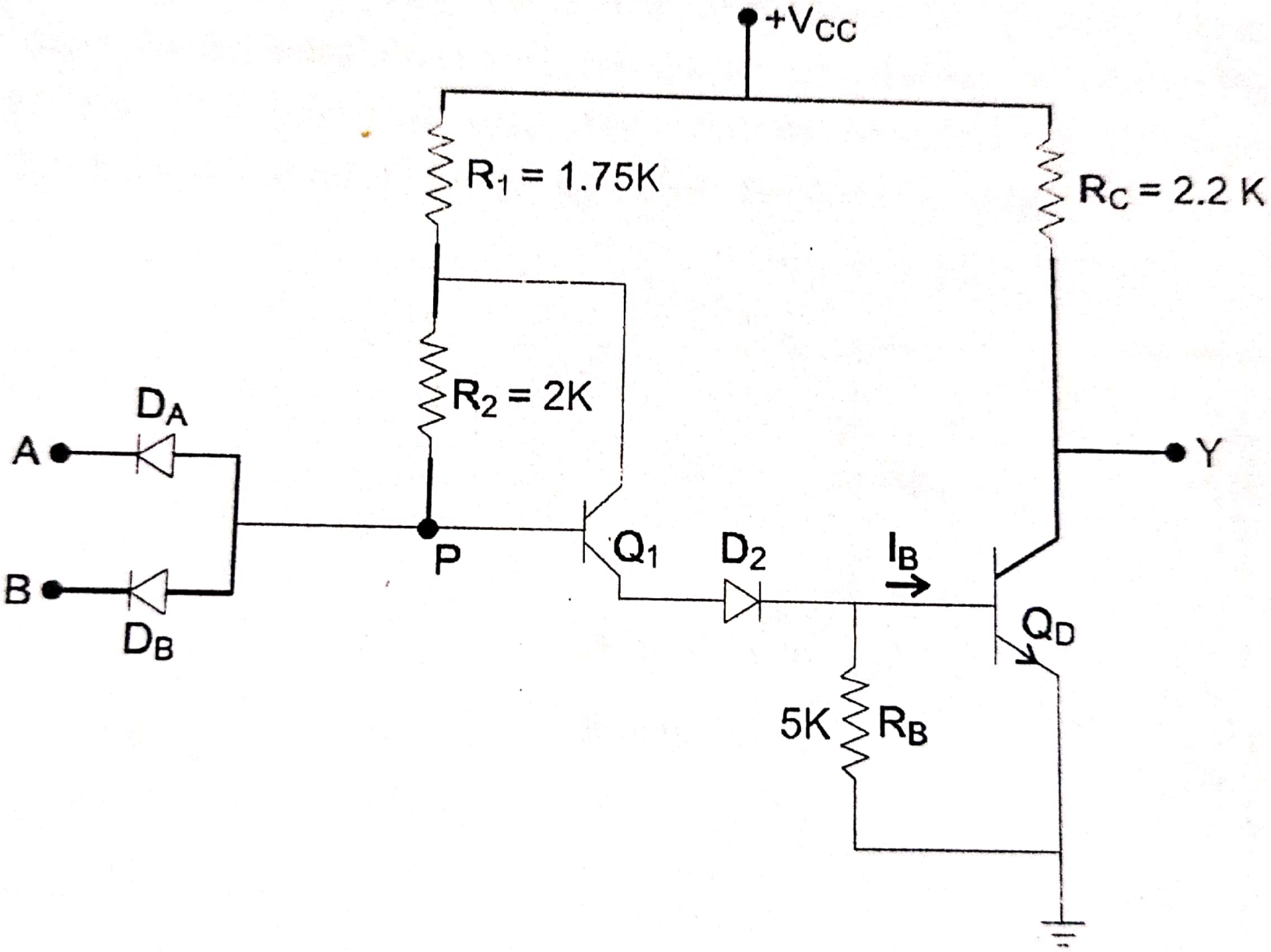


Fig. 10.45 Modified DTL NAND gate

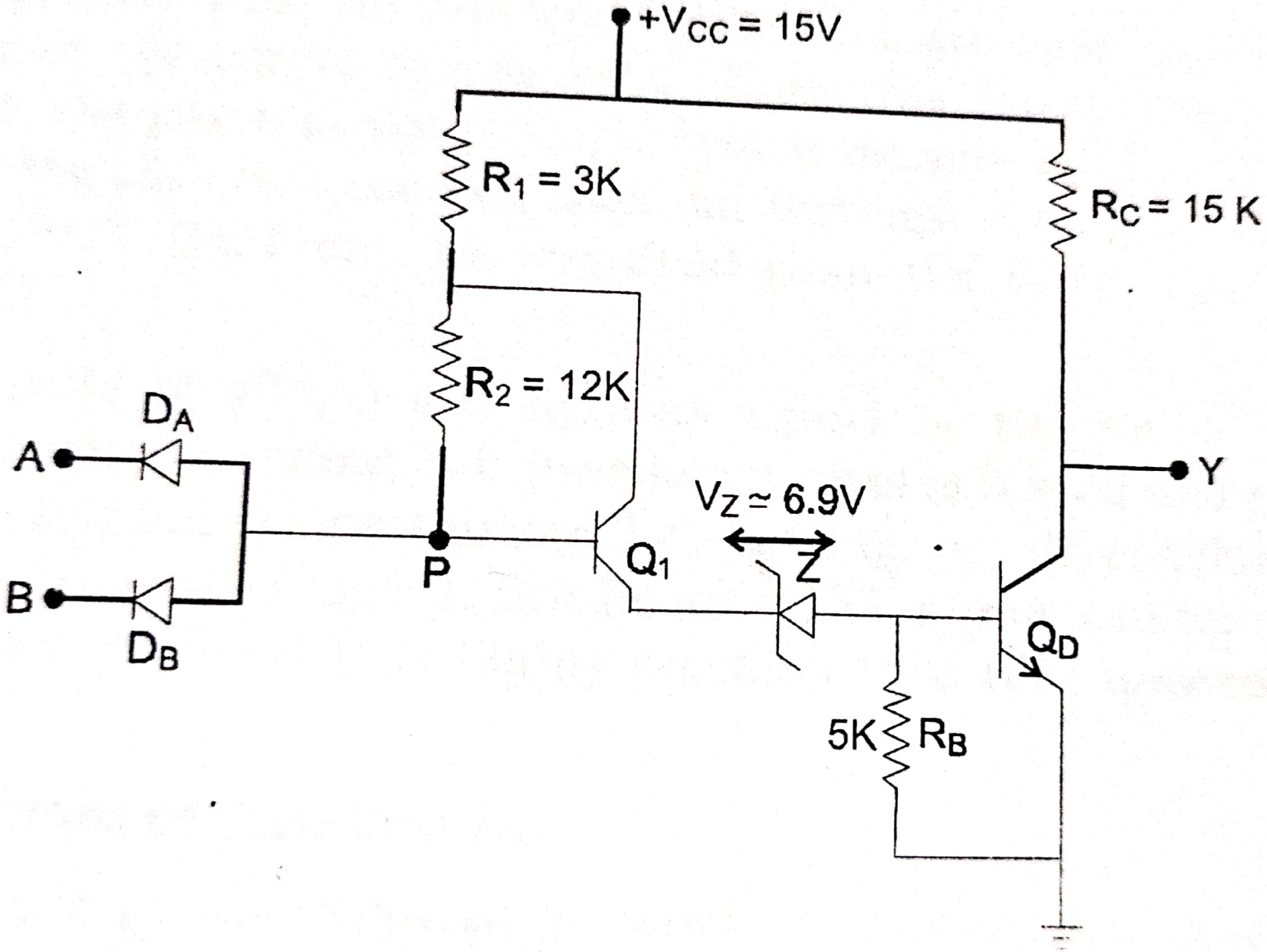


Fig. 10.46 Basic HTL NAND GATE

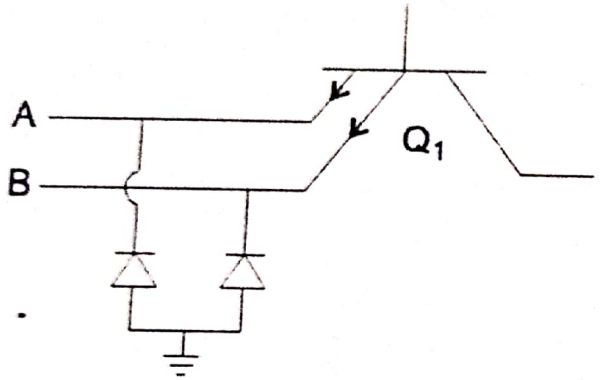


Fig. 10.48 Clamping diodes at input

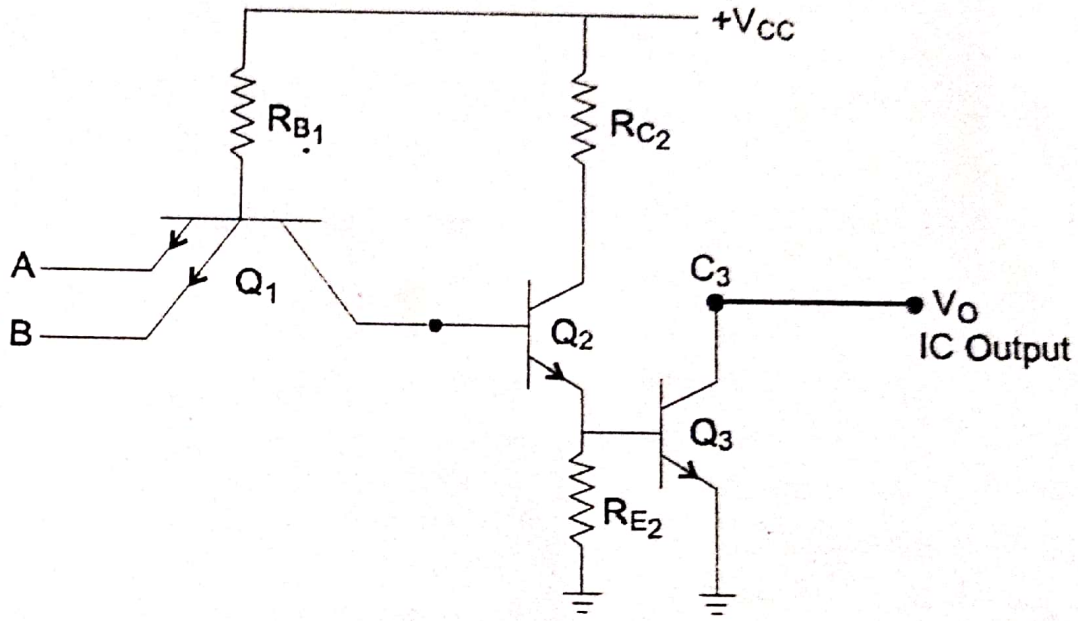


Fig. 10.49 Open collector output of TTL

Open collector output When the collector resistance R_{C_3} of Fig. 10.47 is removed and collector of output transistor Q_3 is made available directly as IC pin, the output is called open collector output. However these outputs must be connected to $+V_{CC}$ through an external resistor, before taking the output.

device) provides the charging current to output capacitance C_O, the circuit shown in Fig. 10.52 is called as active pullup circuit, and the output is called **active pullup output.** Also note that transistors Q_4 and Q_3 forms a totem-pole pair, and hence the output is also called as **totem pole output.** Transistor Q_2 acts as phase splitter for totem pole transistor pair. Advantage of active pullup is increased speed without increasing power dissipation. The purpose of using Diode D is to keep transistor Q_4 in cutoff when output of gate is LOGIC O.

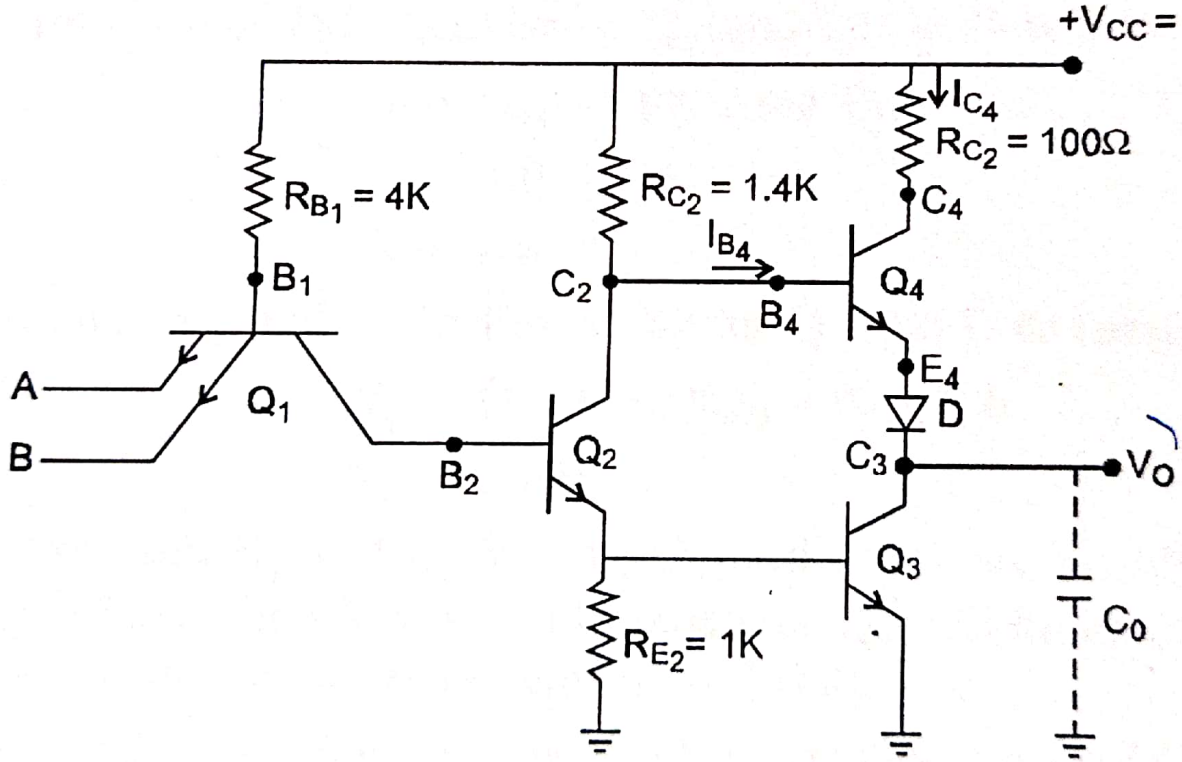
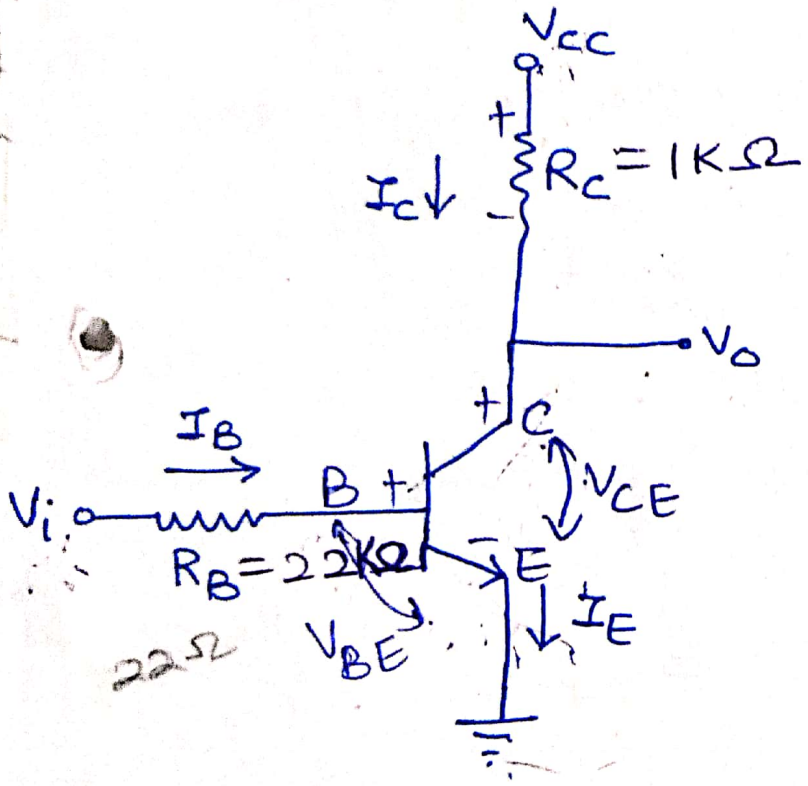
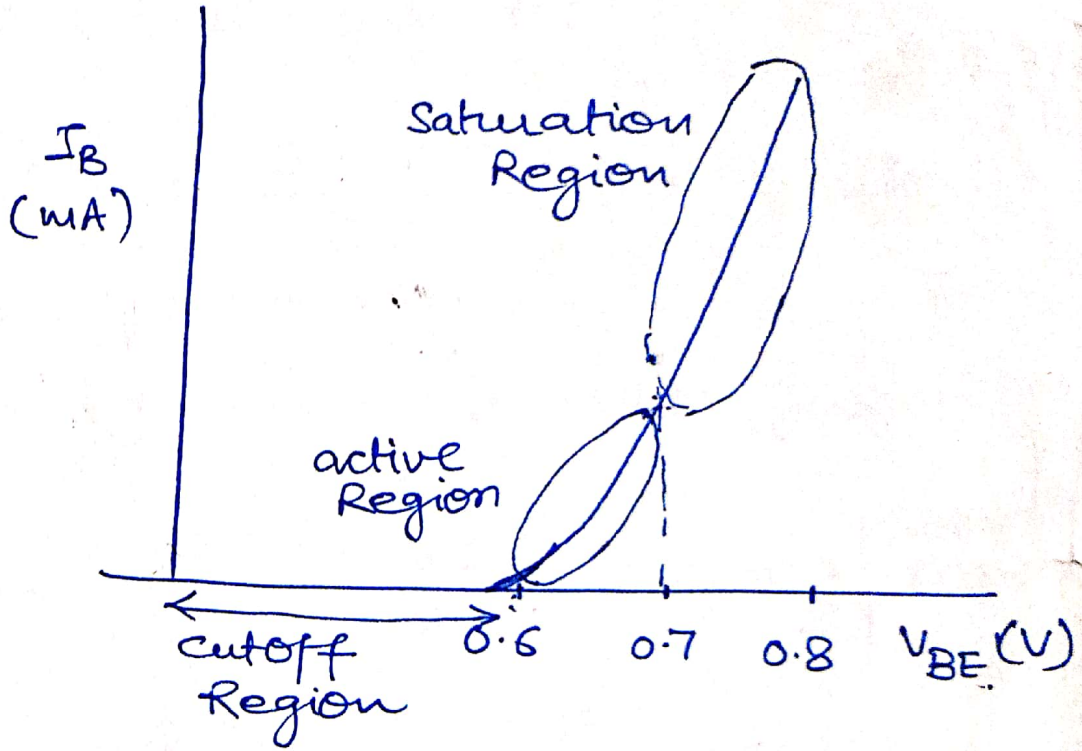


Fig. 10.52 TTL NAND Gate with Active Pullup.

(1.) Bipolar Junction Transistor



(i) Inverter Circuit



(ii) Transistor Base Characteristics

→ When Base-emitter voltage V_{BE} is less than 0.6V, the transistor will be in CutOff and in this case, no Base current will flow.

How it works as an Inverter

→ when input voltage, V_i = L = 0.2V, we have $V_{BE} < 0.6V$ and the transistor is cutOff. The collector-emitter circuit behaves like an open circuit; so output voltage V_o = 5V = H

→ when input voltage, V_i = H = 5V, we have $V_{BE} > 0.6V$.

Let V_{BE} = 0.7, then the Base Current:

$V_i - V_{BE} = I_B R_B$ using KVL

$$I_B = \frac{V_i - V_{BE}}{R_B} = \frac{5 - 0.7}{22\Omega} = 0.195\ mA$$

Let V_{CE} = 0.2V, then the Maximum collector Current:

$V_{CC} - V_{CE} = I_{CS} R_C$ using KVL

$$I_{CS} = \frac{V_{CC} - V_{CE}}{R_C} = \frac{5 - 0.2}{1K\Omega} = 4.8\ mA$$ Saturation Current

Then for Saturation:

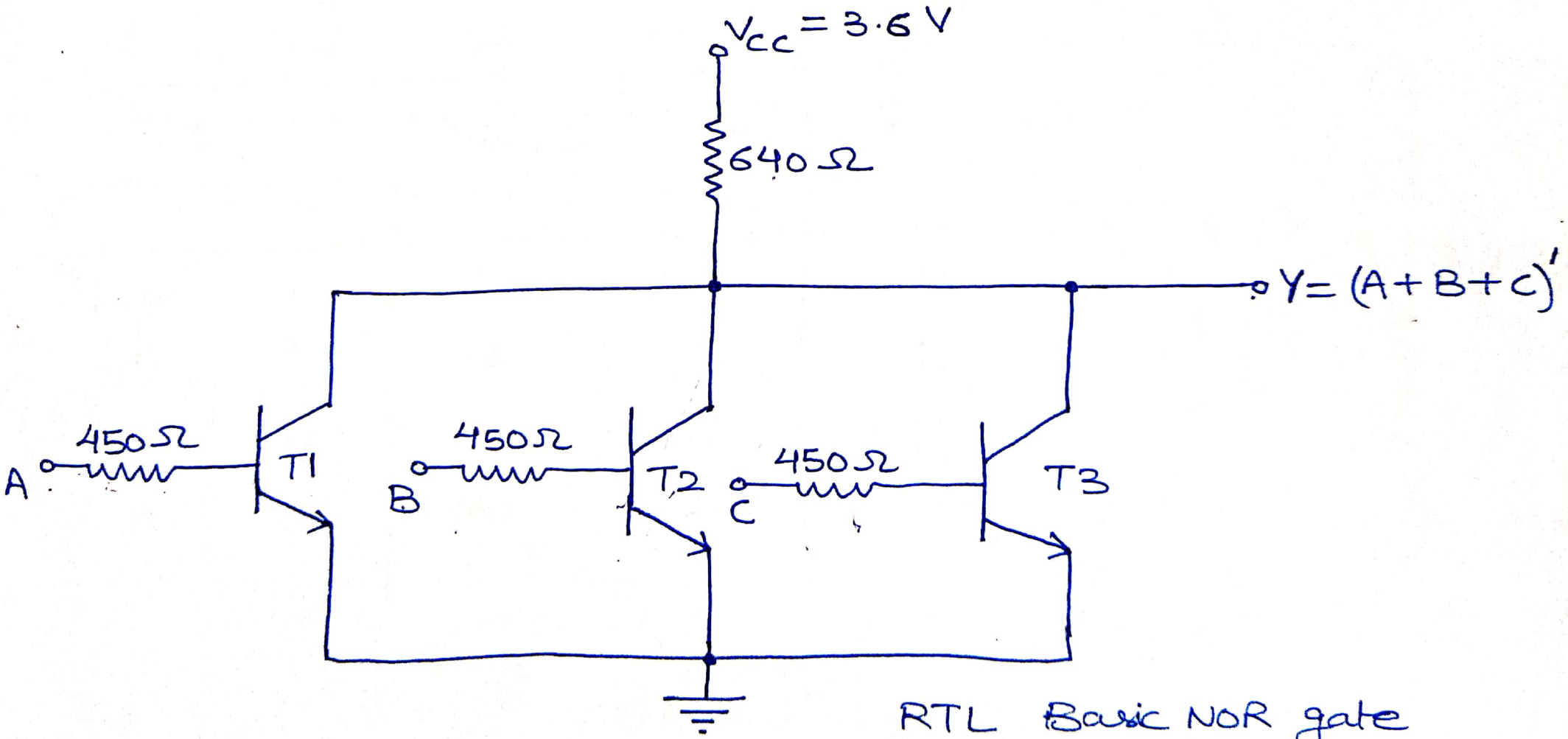
$$0.195 = \boxed{I_B \geq \frac{I_{CS}}{h_{FE}}} = \frac{4.8}{50} = 0.096\ mA$$

(0.195 ↓ from above calculation; $\frac{I_{CS}}{h_{FE}}$ → required)

⇒ the above inequality is satisfied since 0.195 > 0.096

(2.) RTL Basic Gate

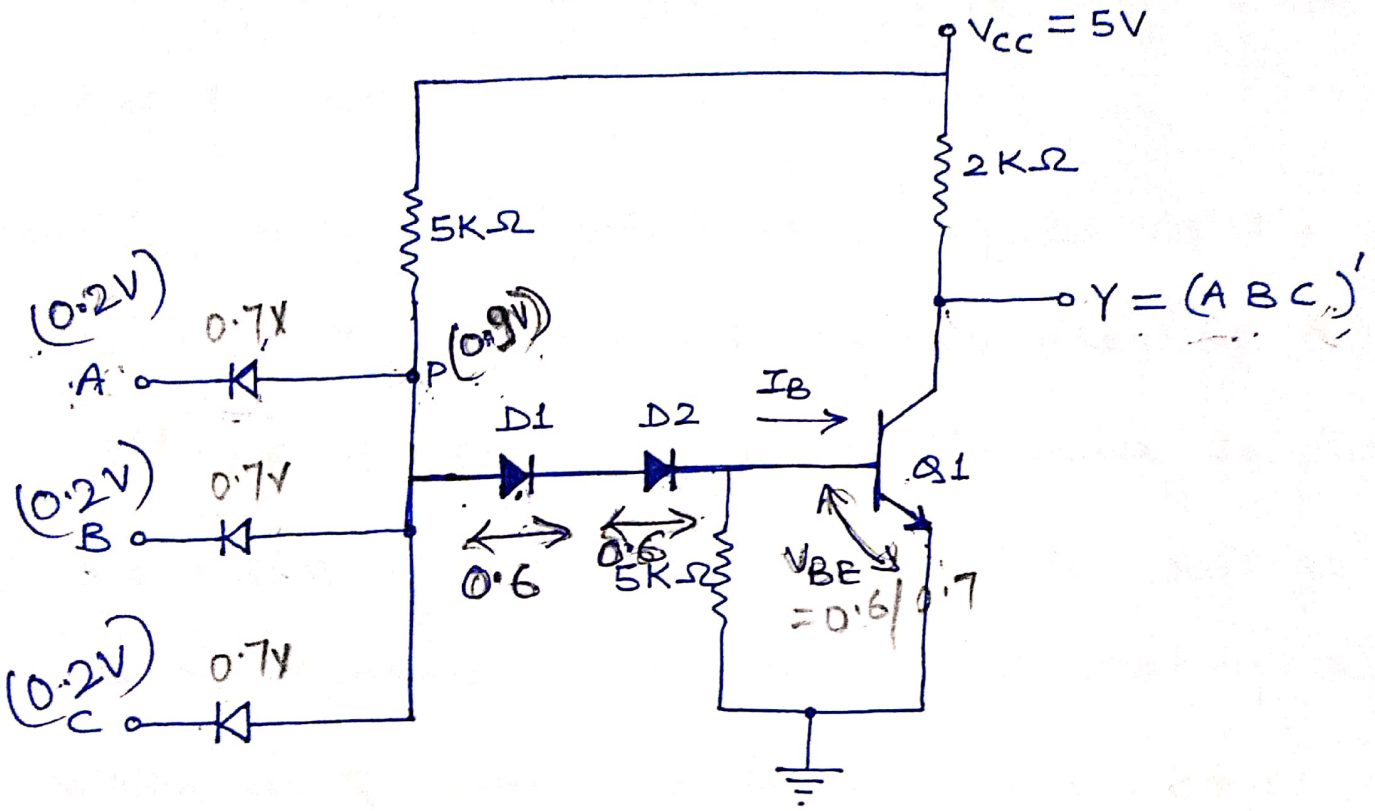
- Resistor-Transistor Logic



RTL Basic NOR gate

(3.) DTL Basic Gates

Diode-Transistor Logic



DTL Basic NAND Gate

Voltage levels for the circuit:

0.2 V for Low-Level

4 to 5 V for High-level

ansistor-Transistor Logic (TTL)

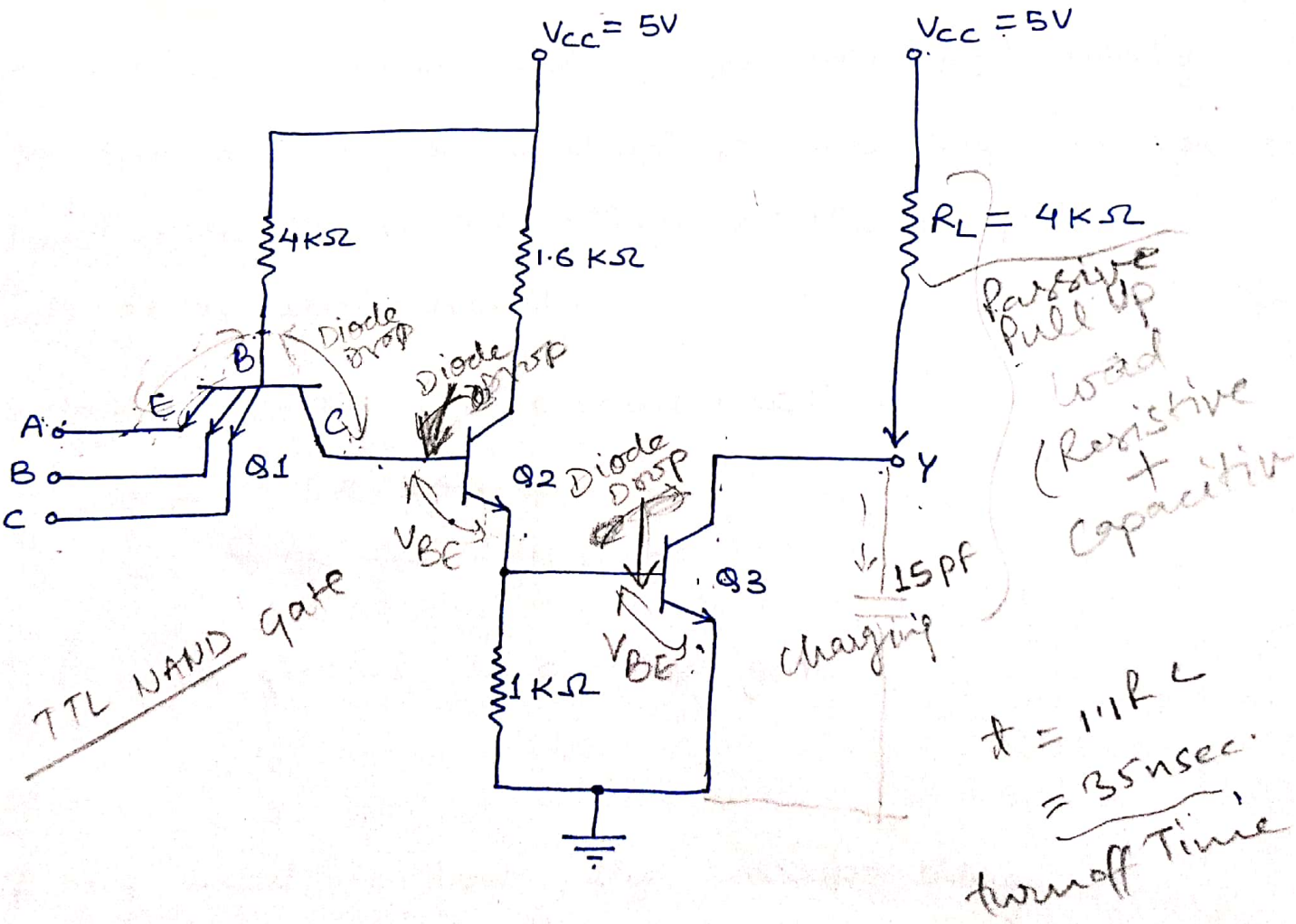
Three TTL types according to output configuration:

(i) Open collector output

(ii) Totem-pole output

(iii) Three-State (or Tri-state) output.

Open Collector Output TTL Gate



→ Multiple Emitters in transistor Q1 are connected to the inputs. These emitters behave like the input diodes in the DTL gate since they form a pn junction with their Base common.

Truth-Table

Inputs		Transistor-States			output
A	B	Q1	Q2	Q3	Y
L	L	ON*	OFF	OFF	H
L	H	ON*	OFF	OFF	H
H	L	ON*	OFF	OFF	H
H	H	OFF	ON	ON	L

*Emitter-Base Junction is forward-Biased.

Totem-Pole output TTL Gate

→ The output impedance of a gate is normally a resistive plus a capacitive load. The capacitive load consists of the capacitance of output transistor, the capacitance of the fan-out gates and any stray wiring capacitance.

→ When the output changes from the low to the high state, the output trasistor of the gate goes from saturation to cutoff and the total load capacitance, C, charges exponentially from the low to the high voltage level with a time constant equal to RC.

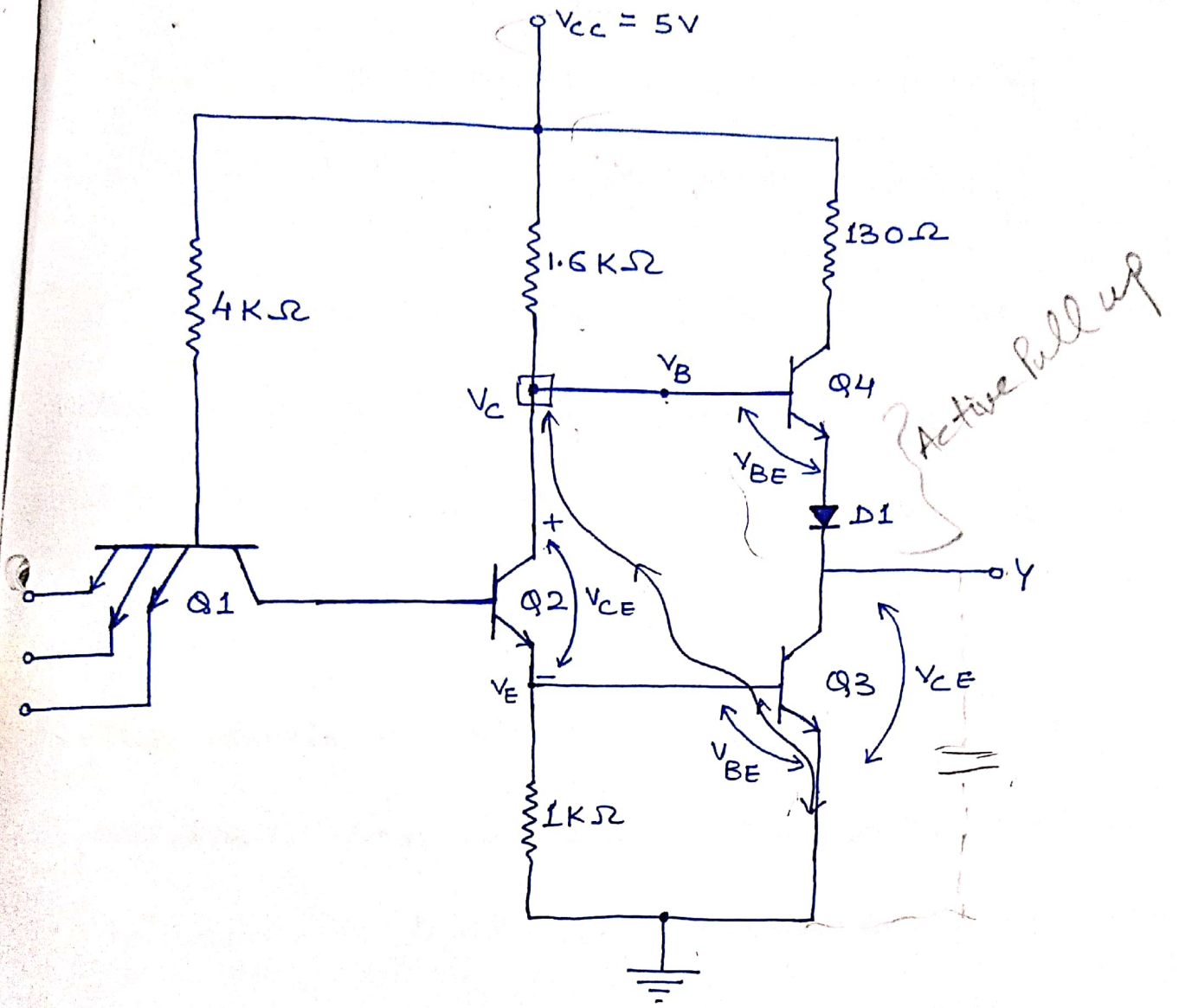
(Q3 ON) → Sat
(Q3 OFF) → Cutoff

→ For the open-collector circuit, typical operating value of C = 15 pF and R_L = 4KΩ, the propagation delay of a TTL open-collector gate during the turn-off time is 35 ns.

→ Now, with an active pull-up circuit replacing the passive pull-up resistor R_L, the propagation-delay will be reduced to 10 ns.

→ This circuit is named as Totem-pole because of the configuration where transistor Q4 "sits" upon transistor Q3.

TTL gate with Totem-pole output



→ for this configuration, when the output Y is in the low state, Q2 and Q3 are driven into saturation same as in the open-collector circuit. ($Q_3 \rightarrow ON \rightarrow$ Sat^n)

→ The voltage in the collector of Q2 will be

$V_{BE}(Q3) + V_{CE}(Q2) \Rightarrow 0.7 + 0.2 = 0.9\,V$.

The output Y will be equal to $V_{CE}(Q3) = 0.2V$

→ Transistor Q4 is cutoff because its base must be one V_{BE} drop plus one diode drop.

⇒ $2 \times 0.6 = 1.2\,V$, to start conducting.

→ Now, since the collector of Q2 is connected to the base of Q4, the voltage in Q4 is only 0.9V instead of the required 1.2V and so Q4 is cutoff.

→ The diode is placed in the circuit to provide a diode drop in the output path and so as to ensure that Q4 is cutoff when Q3 is saturated.

→ Now, when the output changes to the high-state because one of the inputs drops to the low state, transistors Q2 and Q3 will go into cutoff.

→ But, the output will remain in low state momentarily because the voltage across the load capacitance will not change instantaneously.

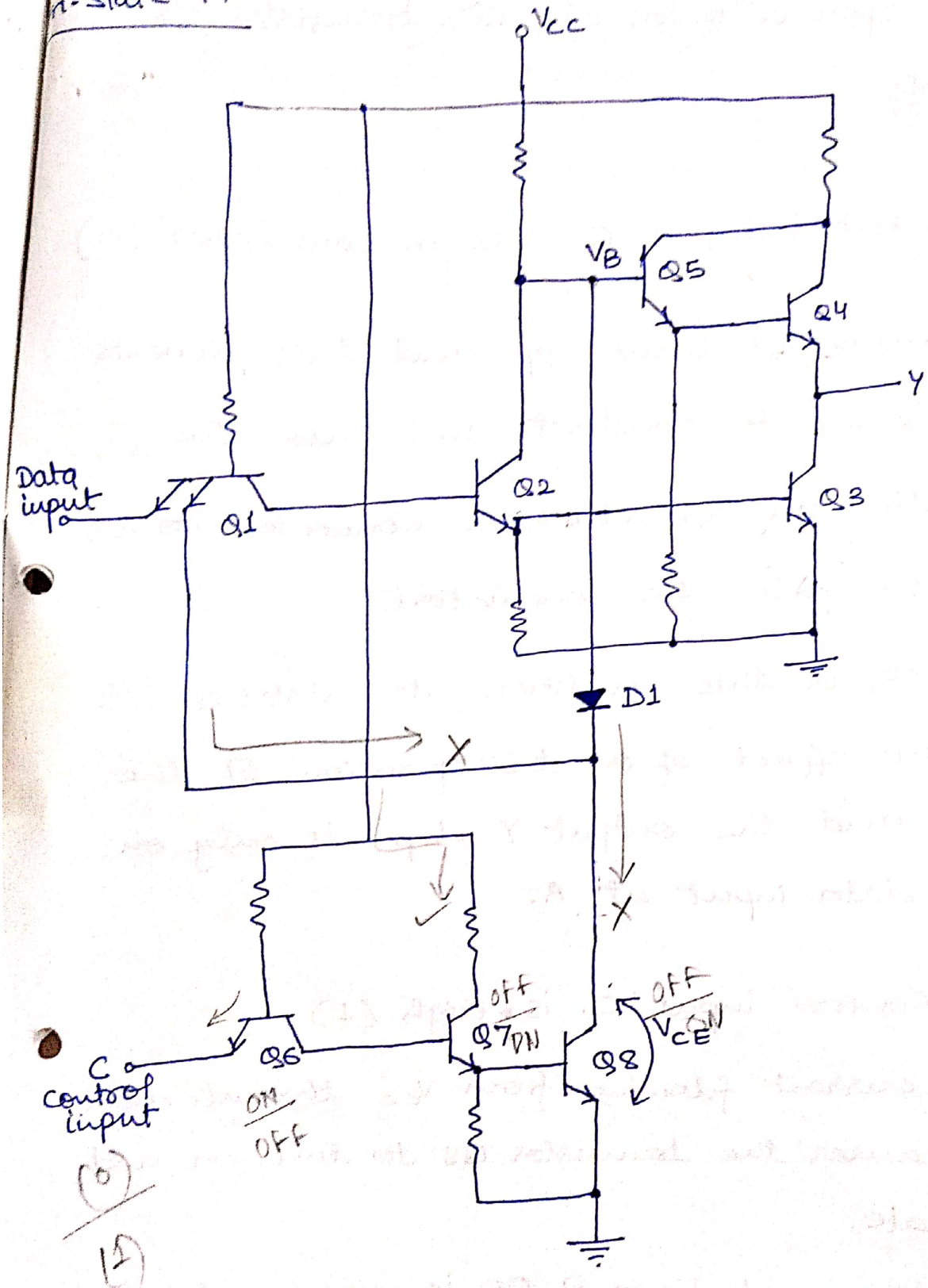
→ Now, as soon as Q2 turns off, Q4 ~~cont~~ will conduct because its base is connected to V_{CC} through the 1.6 KΩ resistor.

→ The current needed to charge the load-capacitance causes Q4 to momentarily saturate, and the output voltage rises with a time-constant RC.

→ But in this case, R (total load resistance) will be equal to 130Ω, plus the saturation resistance of Q4, plus the resistance of the diode, i.e. a total of approximately 150Ω.

→ This value of R (150Ω) is much smaller than the passive pull-up resistance (R_L = 4KΩ) used in the open-collector circuit. and as a result, the transition from the low to high level will be much faster.

i-State TTL



- Transistors Q1 to Q5, associated with the data input, form a totem-pole TTL circuit.
- Transistors Q6, Q7 and Q8 associated with the control input. Form a similar circuit as an open-collector gate.

- As an open collector circuit, transistor Q8 turns off

- When control input C → is in low level (0)

  → Transistor Q8 turns off and this prevents diode D1 to conduct and also the emitter in Q1 which is connected to Q8 has no path for conduction.

  → Hence, in this condition, transistor Q8 has no effect of on the operation of the gate and the output Y depends only on the data input at A.

- When control input C is High (1)

  → The current flowing from V_{cc} through diode D1 causes the transistor Q8 to turn-on and saturate.

  → The voltage at base of Q5 is now equal to the voltage across the saturated transistor (V_{CE}) (Q8) 0.2V plus one diode drop (0.7 V). Total (0.9 V).

This voltage turns off Q4 and Q5 since it is less than two V_{BE} drops.

→ At the same time, the low input to one of the emitters of Q1 forces transistor Q3 and transistor Q2 to turn off.

Now, as Q3 and Q4 in the totem-pole are turned off and the output of the circuit behaves like an open circuit with very high impedance.

Logic

- MOSFETs are very popular due to high density of fabrication and low power dissipation.
- Both p-channel (PMOS) and n-channel (NMOS) devices are used.
- It is also possible to fabricate enhancement mode p-channel and n-channel MOS devices on the same chip. Such devices are reffered to as complementary MOSFETs and logic based on these devices is known as CMOS logic. The power dissipation is extremely small for CMOS.

Basic MOS circuit as an Inverter

→ Driver Circuit can only be an Enhancement MOSFET.

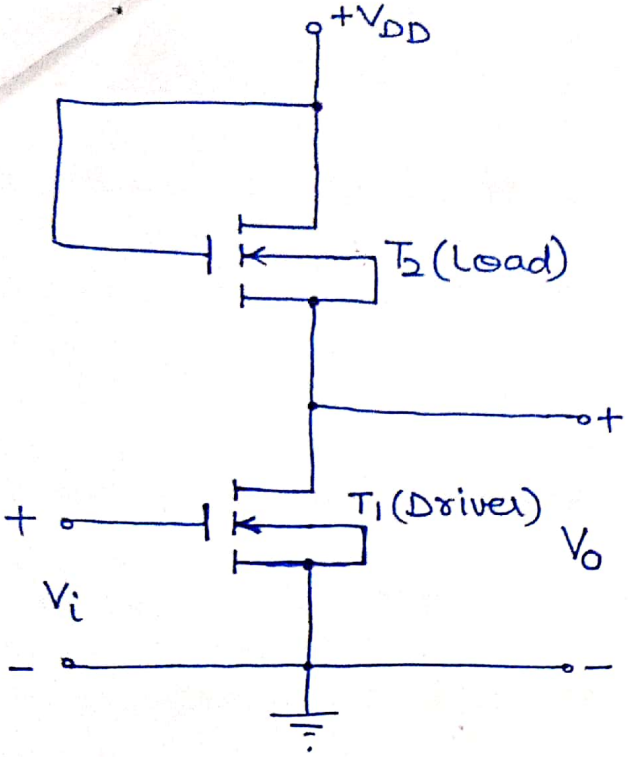
→ Load Circuit may be an Enhancement or Depletion MOSFET.

→ The logic levels for MOS circuits are

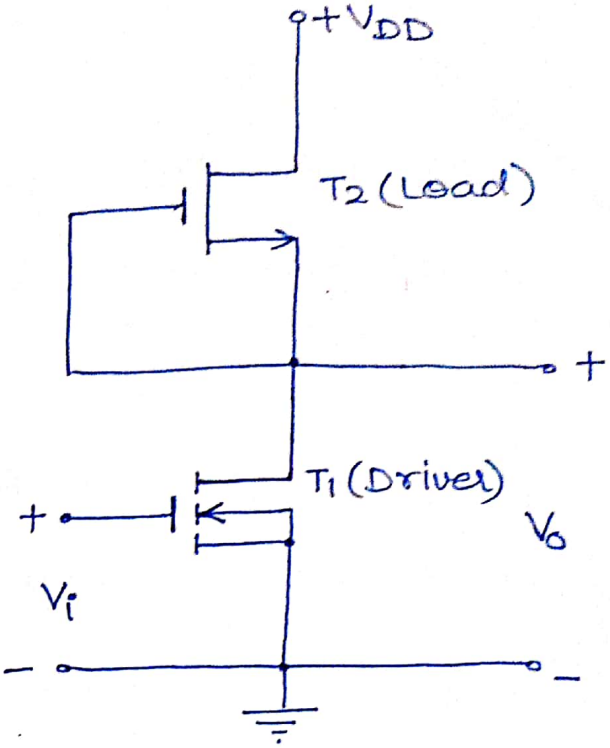
$$V(0) \approx 0$$

$$V(1) \approx V_{DD} \text{ (Drain Voltage)}$$

el Circuit

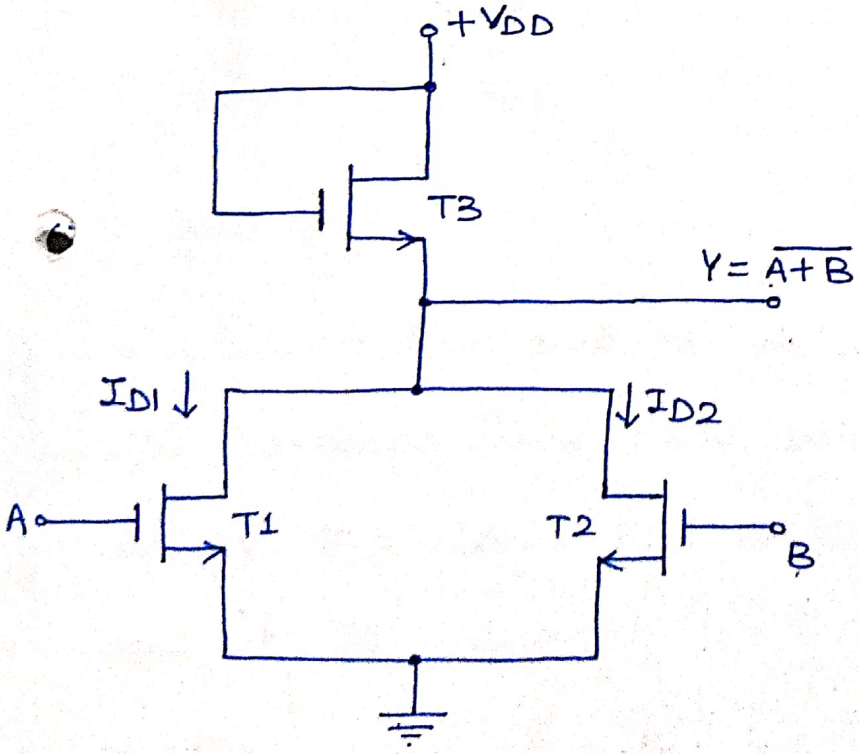


(a) Enhancement Load

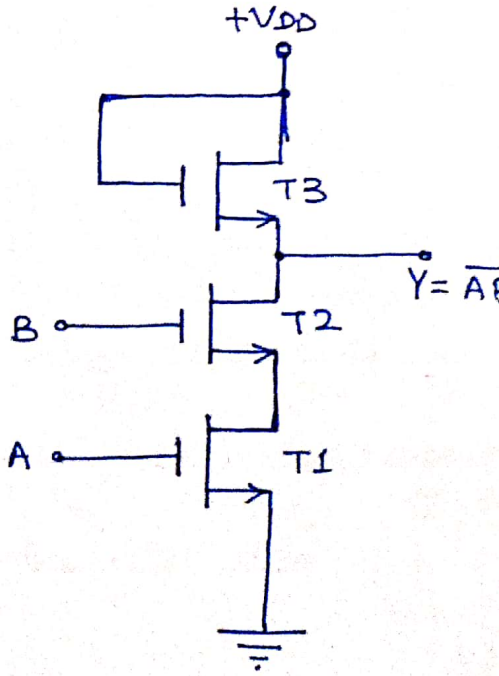


(b) Depletion Load

MOSFET NAND and NOR Gates



2-Input NMOS NOR-gate



2-Input NMOS NAND-gate

NOR Gate

→ When Both inputs are 0 (Low), both transistors T1 and T2 are OFF ($I_{D1} = I_{D2} = 0$) and hence the output is V_{DD}.

→ When either one or both of the inputs are $V(1) = V_{DD}$ (High), the corresponding FETs will be ON and the output is 0 V.

Inputs		output
A	B	Y
0	0	V_{DD}
0	V_{DD}	0
V_{DD}	0	0
V_{DD}	V_{DD}	0

ii) NAND Gate

→ when either one or both inputs are $V(0) = 0$ (Low) the corresponding FETs will be OFF, the voltage across the load FET will be 0, hence the output is V_{DD}.

→ When both inputs are $V(1) = V_{DD}$ (High), both T1 and T2 are ON and the output is 0.

Complementary MOSFET (CMOS)

→ The n-channel MOS conducts when its gate-to-source voltage is positive.

→ The p-channel MOS conducts when its gate-to-source voltage is negative.

→ Either type of device is turned off if its gate-to-source voltage is zero.

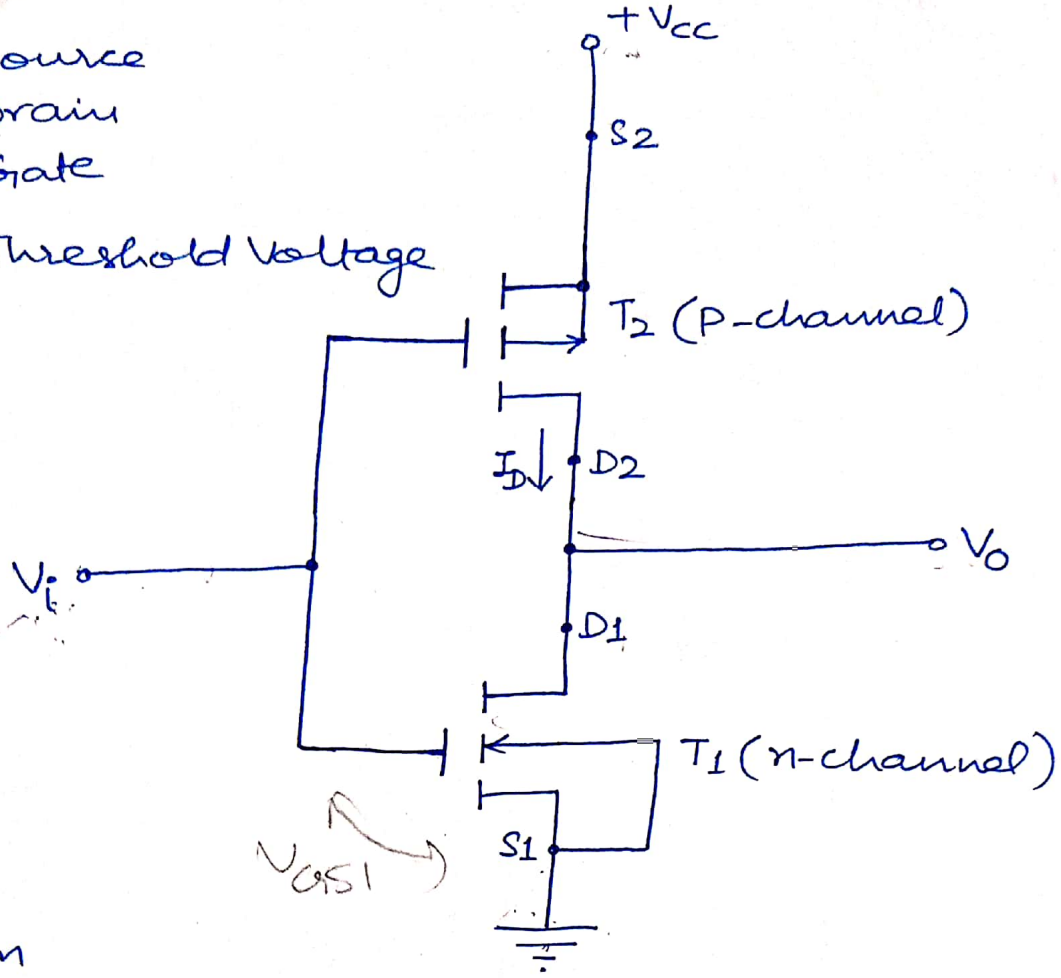
→ A complementary MOSFET (CMOS) is obtained by connecting a p-channel and an n-channel MOSFET in series, with drains tied together and the output is taken at the common drain point. Input is applied at the common-gate connection formed by connecting the two gates together.

(i) C-MOS Inverter

→ Logic levels are 0 V (logic 0)

V_{cc} (logic 1)

S → Source
D → Drain
G → Gate
V_T → Threshold Voltage



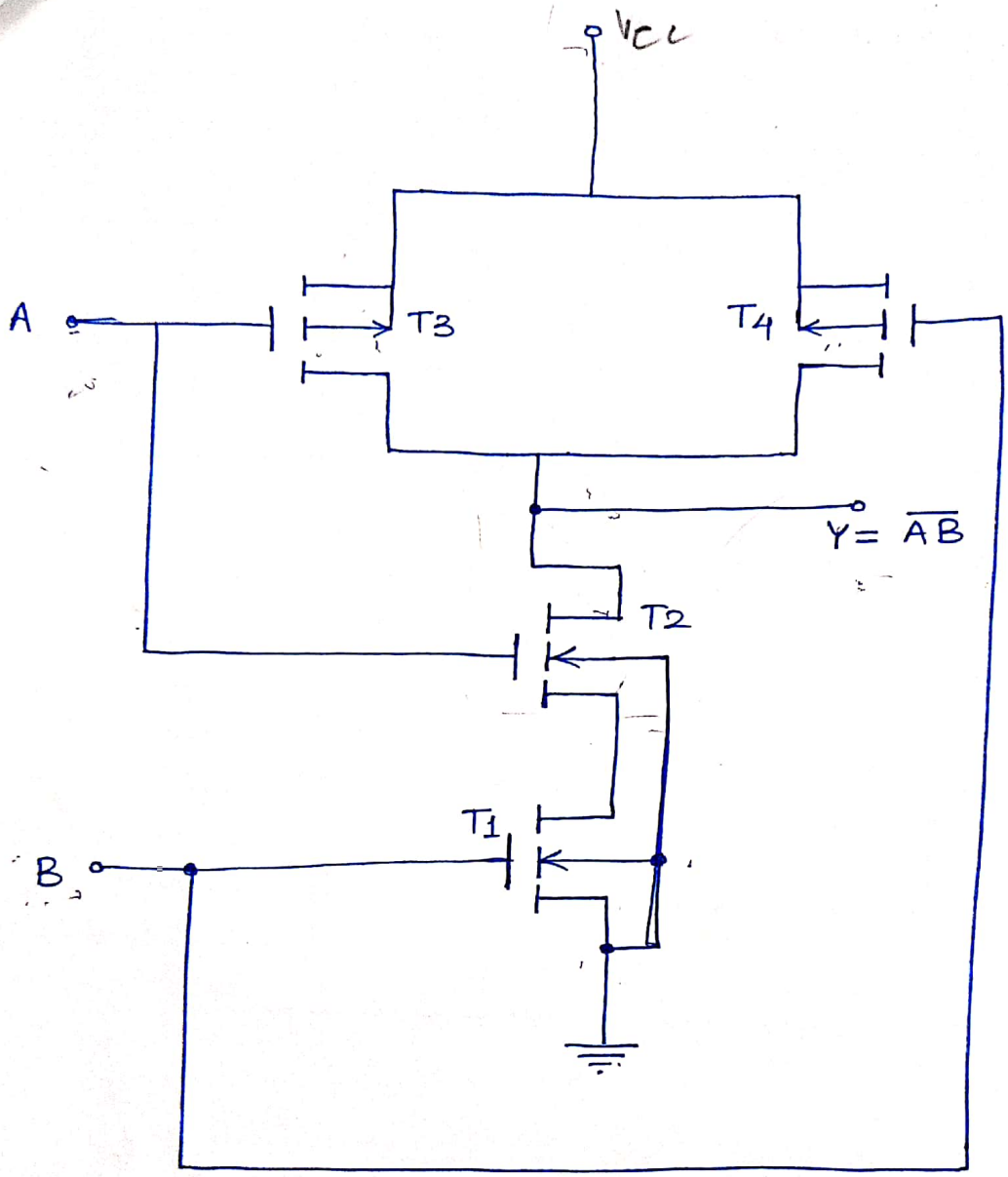
operation

→ when $V_i = V_{CC}$ (High), T_1 turns ON ($V_{GS1} > V_T$) and T_2 is OFF since $V_{GS2} = 0V$.

Therefore $V_o \approx 0V$ and since the transistors are connected in series, the current I_D will be the drain current of the OFF transistor T_2 which is negligibely small.

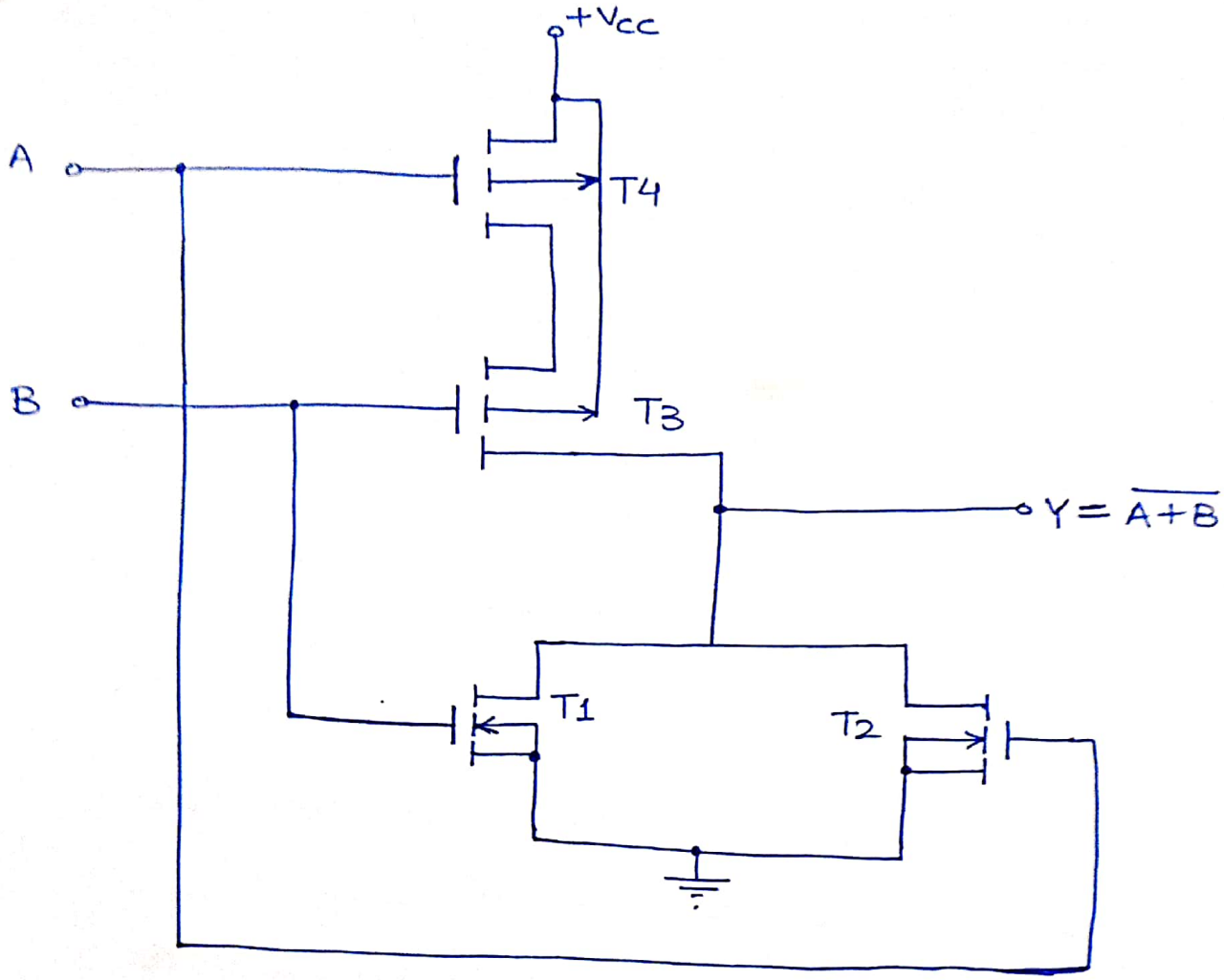
→ when $V_i = 0V$ (LOW), T_1 turns off ($V_{GS1} < V_T$) and T_2 turns ON ($|V_{GS2}| > |V_T|$) which gives an output voltage $V_o \approx V_{CC}$ and again I_D is very small being the drain current of the off transistor T_1.

of CMOS NAND-Gate



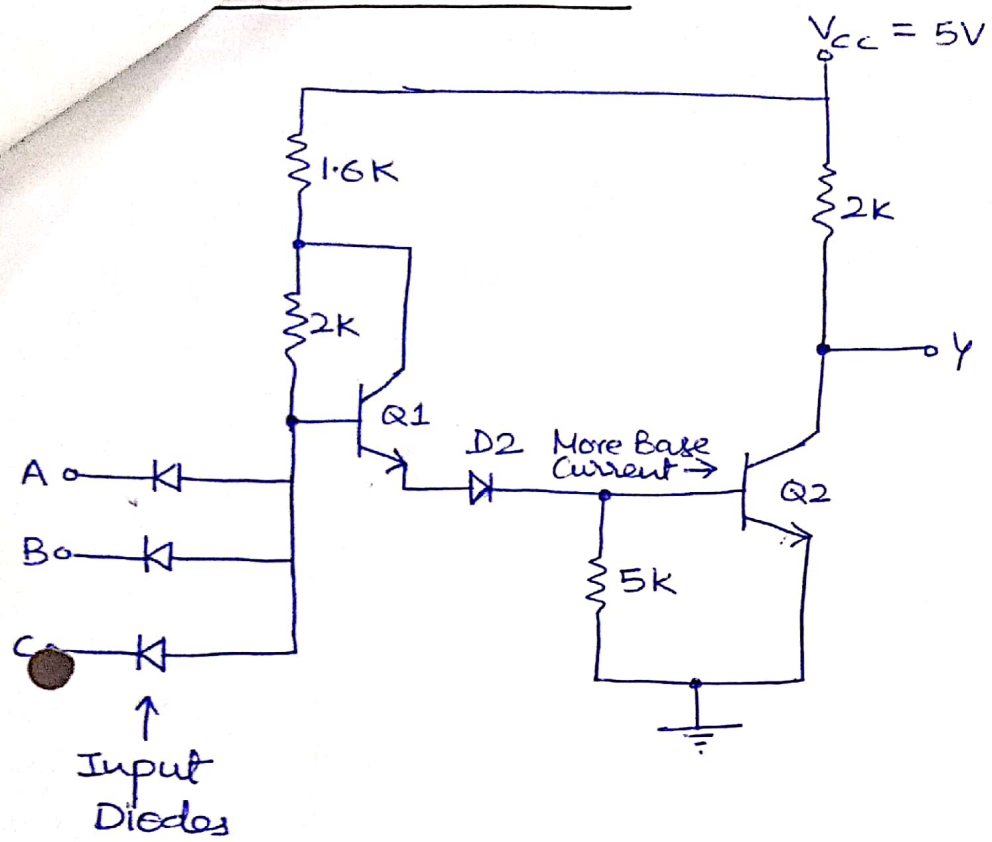
Input		State of MOS Devices				Output
A	B	T1	T2	T3	T4	Y
0	0	OFF	OFF	ON	ON	V_{cc}
0	V_{cc}	ON	OFF	ON	OFF	V_{cc}
V_{cc}	0	OFF	ON	OFF	ON	V_{cc}
V_{cc}	V_{cc}	ON	ON	OFF	OFF	0

... of CMOS NOR-Gate



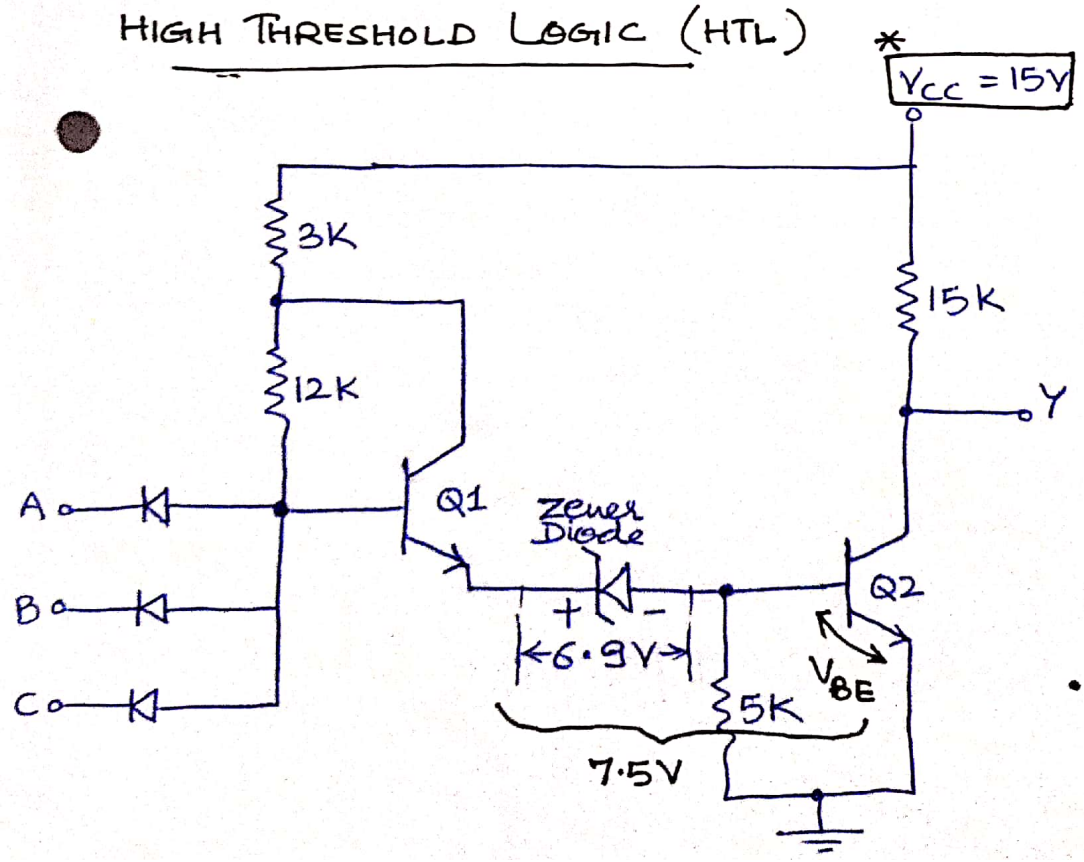
Inputs		State of MOS Devices				output
A	B	T1	T2	T3	T4	Y
0	0	OFF	OFF	ON	ON	V_{cc}
0	V_{cc}	ON	OFF	OFF	ON	0
V_{cc}	0	OFF	ON	ON	OFF	0
V_{cc}	V_{cc}	ON	ON	OFF	OFF	0

IFIED DTL Gate



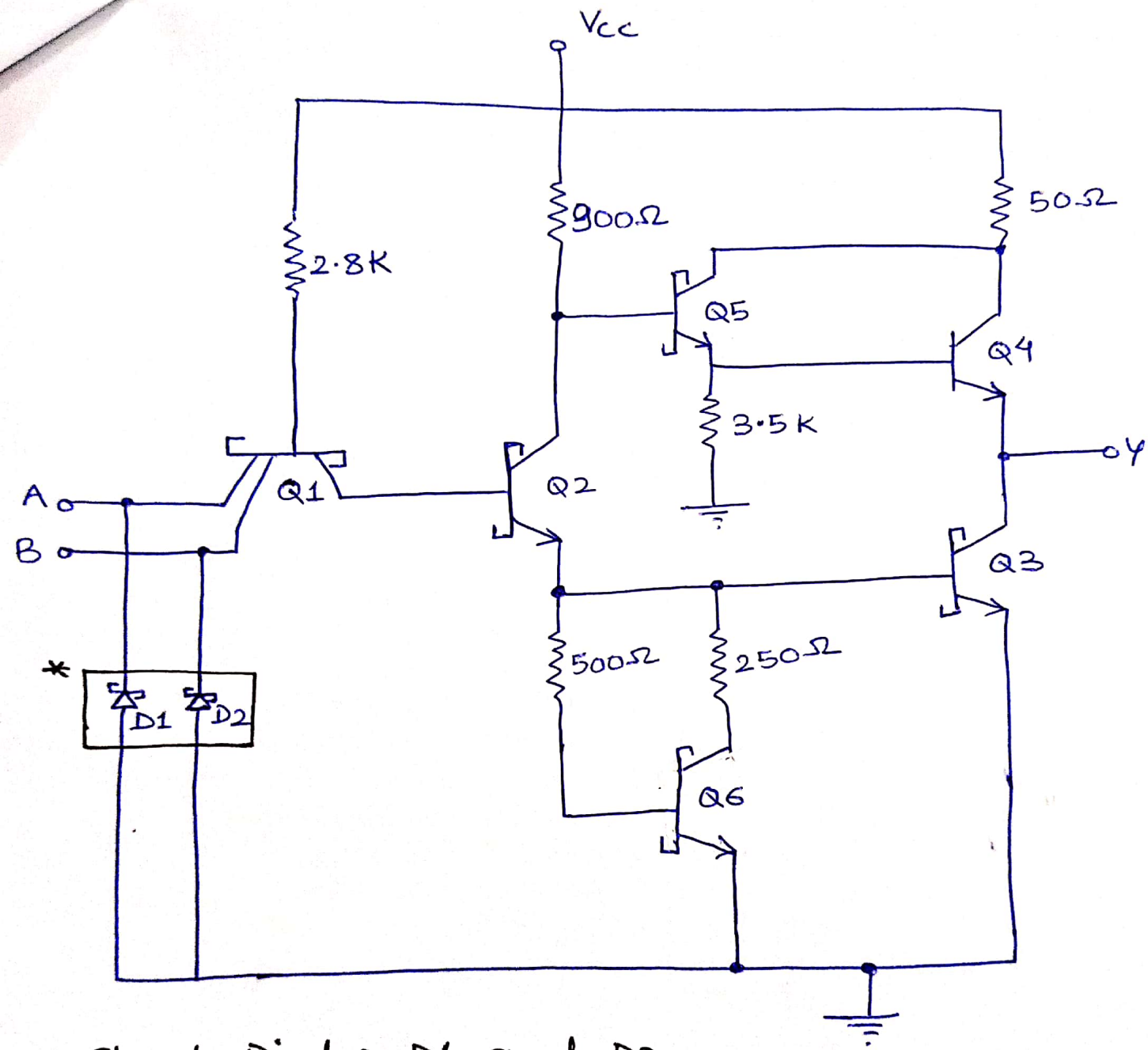
- Improved fan-out as Transistor Q1 is maintained in the active region when o/p transistor Q2 is saturated.

HIGH THRESHOLD LOGIC (HTL)



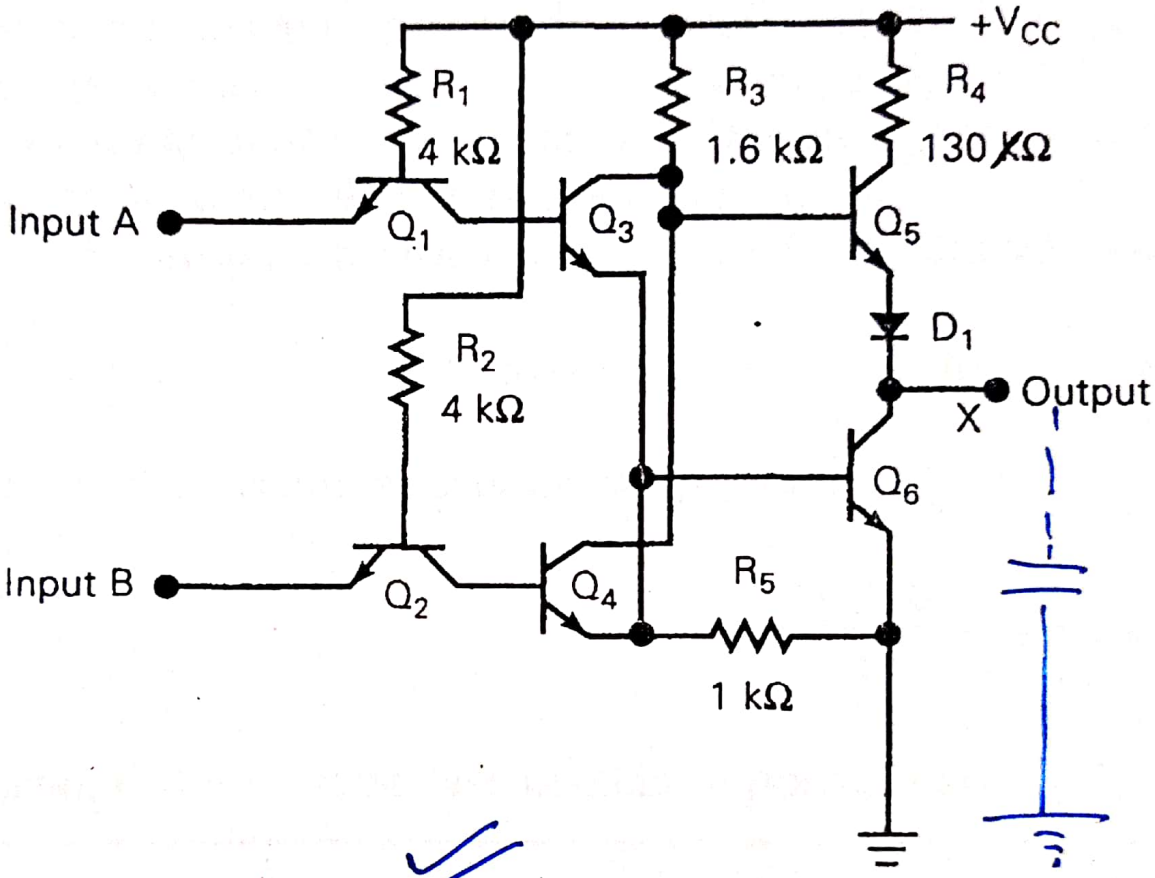
- For improved noise-immunity
- Noise signal must be > 7.5 V to change the state of Q2.
- Low Level → 0.2 V
  High Level → 15 V

TTL Gate



* Shunt Diodes D1 and D2 are present to limit negative input voltages.

TTL NOR gate



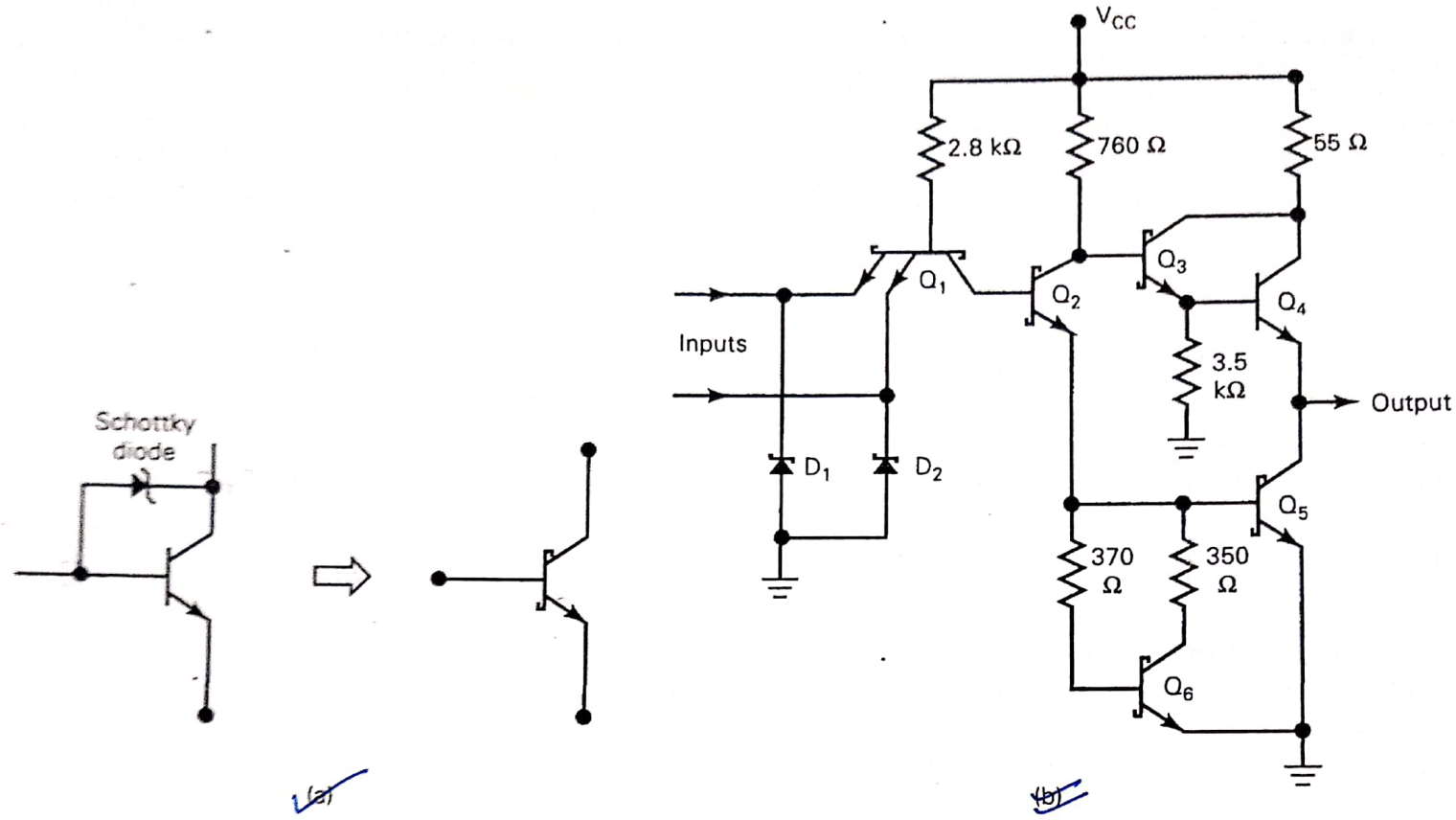


FIGURE 8-12 (a) Schottky-clamped transistor; (b) basic NAND gate in S-TTL series. (Courtesy of Fairchild, a Schlumberger company)