Jaipur Engineering College & Research Centre, Jaipur

Lecture Notes

3EE4-06: Analog Electronics

ACADEMIC SESSION 2020-21

Prepared By:
Jisha Varghese

VISION OF ELECTRICAL ENGINEERING DEPARTMENT

Electrical Engineering Department strives to be recognized globally for outcome based knowledge and to develop human potential to practice advance technology which contribute to society.

MISSION OF ELECTRICAL ENGINEERING DEPARTMENT

M1. To impart quality technical knowledge to the learners to make them globally competitive Electrical Engineers.

M2. To provide the learners ethical guidelines along with excellent academic environment for a long productive career.

M3. To promote industry-institute relationship.

PROGRAM OUTCOMES

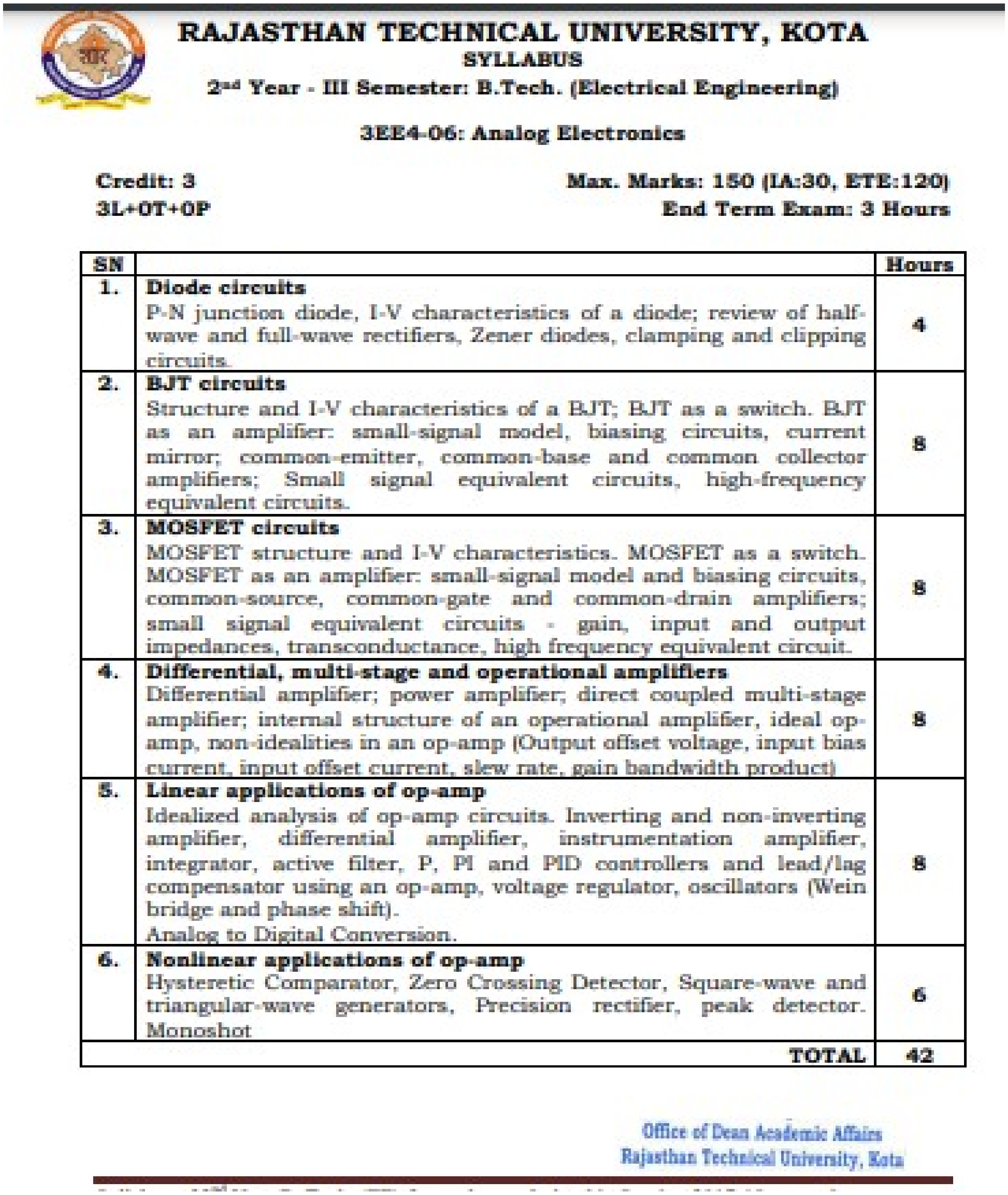
1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems in Electrical Engineering.
2. **Problem analysis:** Identify, formulate, research literature, and analyze complex engineering problems reaching substantial conclusions using first principles of mathematics, natural sciences, and engineering sciences in Electrical Engineering.
3. **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations using Electrical Engineering.
4. **Conduct investigations of complex problems:** Use research based knowledge and research methods including design of experiments, analysis and interpretation of data and synthesis of the information to provide valid conclusions using Electrical Engineering.
5. **Modern tool usage:** Create, select and apply appropriate techniques, resources, and modern engineering and EE tools including prediction and modeling to complex engineering activities with an understanding of the limitations in EE.
6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice using EE.
7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of EE and need for sustainable development in EE.
8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice using EE.
9. **Individual and team work:** Function effectively as an individual and as a member or leader in diverse teams, and multi-disciplinary settings in EE.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations and give and receive clear instructions.
11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage EE projects and in multi-disciplinary environments.
12. **Life-long learning:** Recognize the need for and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological changes needed in EE.

COURSE OUTCOMES:

On successful completion of the course, the students will be able to: -

CO 1	Understand the characteristics of Diodes, concepts behind the Clippers, and Clampers. Design and analysis of various rectifier and amplifier circuits
CO 2	Analyze the characteristics of current flow in a bipolar junction transistor and MOSFET & different electronic devices such as Amplifiers
CO 3	Understand the dynamics of Linear & Non Linear Devices

Syllabus



RAJASTHAN TECHNICAL UNIVERSITY, KOTA

SYLLABUS

2nd Year - III Semester: B.Tech. (Electrical Engineering)

3EE4-06: Analog Electronics

Credit: 3 **Max. Marks: 150 (IA:30, ETE:120)**
3L+0T+0P **End Term Exam: 3 Hours**

SN		Hours
1.	**Diode circuits** P-N junction diode, I-V characteristics of a diode; review of half-wave and full-wave rectifiers, Zener diodes, clamping and clipping circuits.	4
2.	**BJT circuits** Structure and I-V characteristics of a BJT; BJT as a switch. BJT as an amplifier: small-signal model, biasing circuits, current mirror; common-emitter, common-base and common collector amplifiers; Small signal equivalent circuits, high-frequency equivalent circuits.	8
3.	**MOSFET circuits** MOSFET structure and I-V characteristics. MOSFET as a switch. MOSFET as an amplifier: small-signal model and biasing circuits, common-source, common-gate and common-drain amplifiers; small signal equivalent circuits - gain, input and output impedances, transconductance, high frequency equivalent circuit.	8
4.	**Differential, multi-stage and operational amplifiers** Differential amplifier; power amplifier; direct coupled multi-stage amplifier; internal structure of an operational amplifier, ideal op-amp, non-idealities in an op-amp (Output offset voltage, input bias current, input offset current, slew rate, gain bandwidth product)	8
5.	**Linear applications of op-amp** Idealized analysis of op-amp circuits. Inverting and non-inverting amplifier, differential amplifier, instrumentation amplifier, integrator, active filter, P, PI and PID controllers and lead/lag compensator using an op-amp, voltage regulator, oscillators (Wein bridge and phase shift). Analog to Digital Conversion.	8
6.	**Nonlinear applications of op-amp** Hysteretic Comparator, Zero Crossing Detector, Square-wave and triangular-wave generators, Precision rectifier, peak detector. Monoshot	6
	TOTAL	**42**

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Rajasthan Technical University, Kota

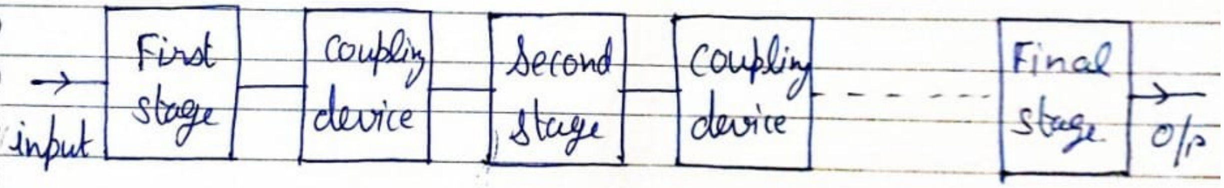
Unit: 4

Chapter: Differential, Multi-stage and Operational Amplifier

Multistage transistor Amplifier (cascaded)

- A transistor circuit containing more than one stage of amplification.

coupling device	Name of amplifier
① No device	Direct coupling
② Resistance and capacitors	R-C coupling
③ Transformer	Transformer coupling

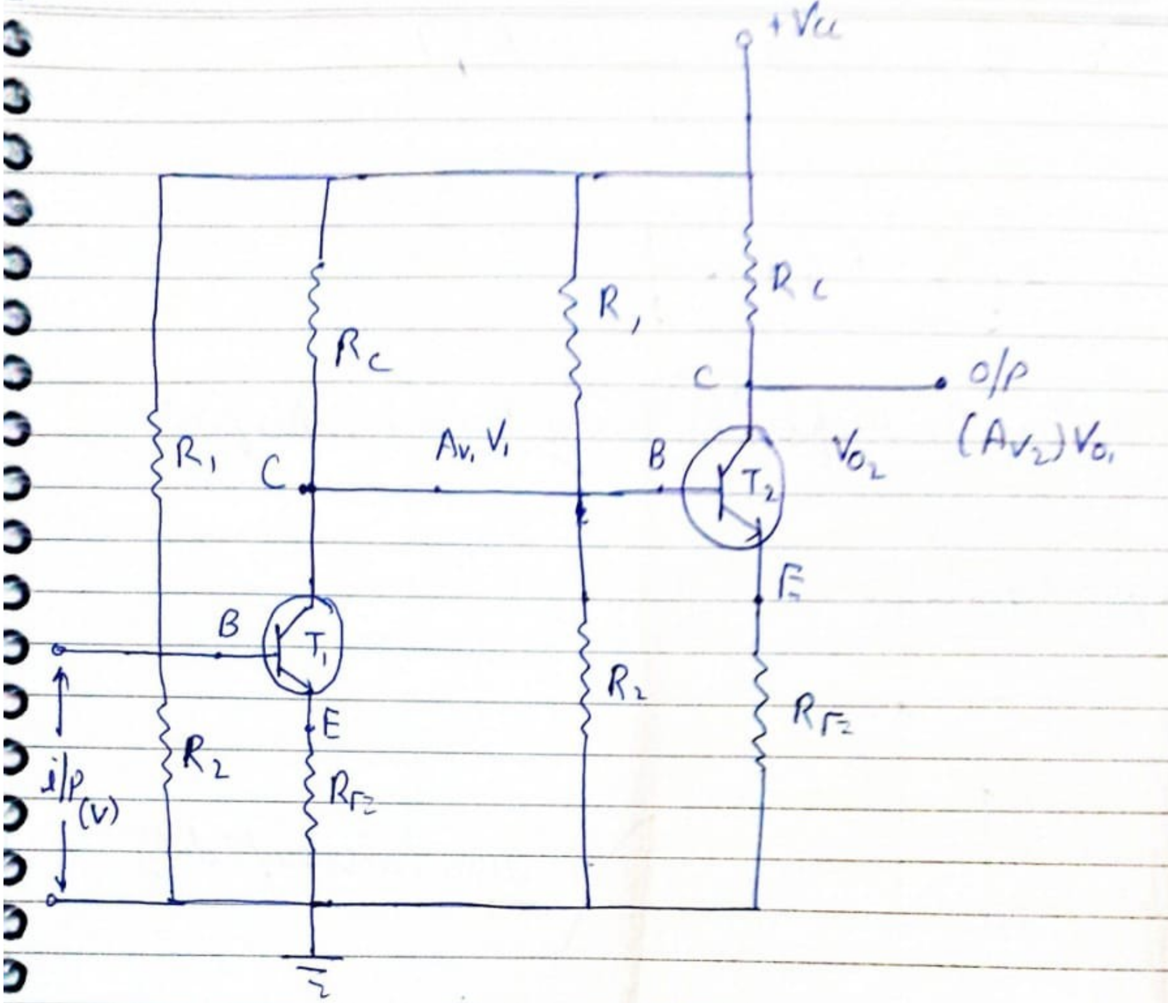


Multistage Amplifier

Direct Coupled (DC) Amplifier :

DC amplifier are used at very low frequency (<10Hz)

The coupling devices (capacitor and transformer) are not used at low freq. (as its size are very large at low freq.).



Two stage CE amplifier, o/p of T_1 is connected to i/p base of transistor T_2. Signal (V_i) is applied at the base T_1, ~~where it is applied at the base of T_1~~.

Let Av_1 be the voltage gain of T_1 and Av_2 be the voltage gain of T_2.

The amplified o/p of T_1 is applied at the base of T_2.

Let V_0 be the o/p

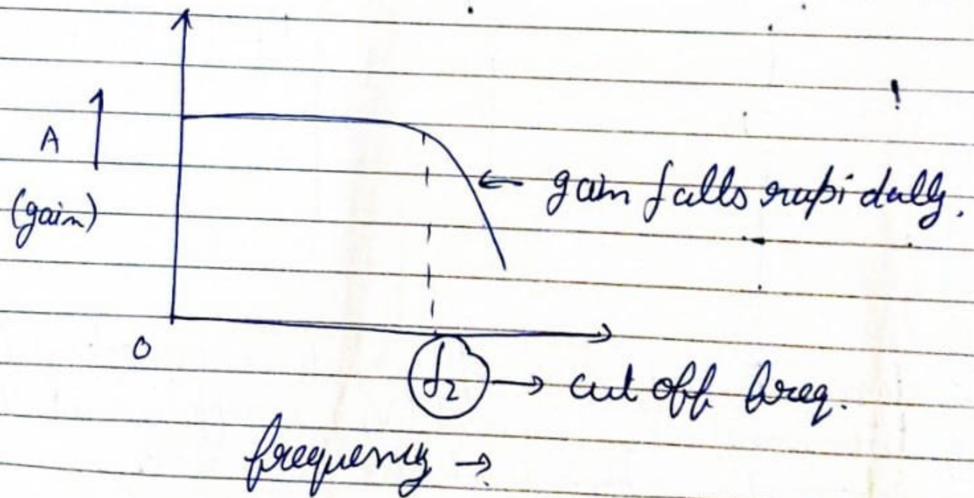
$$\boxed{V_0 = Av_1 \cdot Av_2 \cdot V_i}$$

Voltage gain $A_V = \frac{V_o}{V_i} = A_{V_1} \cdot A_{V_2}$

$$\boxed{A_V = A_{V_1} \cdot A_{V_2}}$$

Hence for DC Amplifier we get an amplified o/p.

Frequency Response.



After cut off frequency, the gain falls rapidally because at higher freq. the transistor capacitance comes into existence and gain decreases.

Applications :- (used when freq. s/g is below 10 Hz)

① ~~Ap~~ Amplifying photo-electric current.

② Amplifying thermocouple current.

Differential ~~Gain~~ (DA) Amplifier

It is used to amplify the difference of two s/g. Signal freq. can vary from DcHz to MHz.

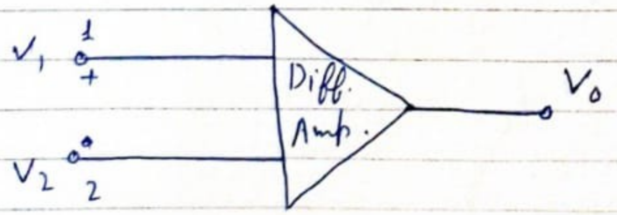
Types of configuration:

1) Dual i/P, balanced o/p differential Amplifier (

2) Dual i/P, unbalanced o/p differential Amplifier.

3) Single i/P, balanced o/p differential Amplifier.

4) Single o/p, unbalanced o/p differential Amplifier



Let V_1 ; V_2 be the two i/p s/g & V_0 be the o/p.

One end is called non-inverting end (terminal-1) and others as inverting end (terminal-2)

Differential Gain (Ad)

Ratio of o/p voltage (V_{o_1}) to difference of i/p voltage at non inverting and inverting terminals.

$$\boxed{A_d = \frac{V_{o_1}}{V_1 - V_2}}$$

$$V_{o_1} = A_d(V_1 - V_2)$$

Common Mode Gain (Ac)

Ratio of o/p voltage (V_{o_2}) to avg. i/p voltage $\frac{(V_1+V_2)}{2}$

$$A_C = \frac{V_{o_2}}{(V_1+V_2)/2}$$

$$\boxed{V_{o_2} = \frac{A_C \cdot (V_1+V_2)}{2}}$$

Let V_o be the final o/p which is sum of two o/ps is i.e. $V_o = V_{o1} + V_{o2}$

$$= A_d (V_1 - V_2) + A_c \frac{(V_1+V_2)}{2}.$$

$$\boxed{V_o = A_d V_d + A_c V_c.}$$

where V_d = difference mode s/g = $(V_1 - V_2)$

V_c = Common mode s/g = $(V_1+V_2)/2$

Common Mode rejection ratio (CMRR)

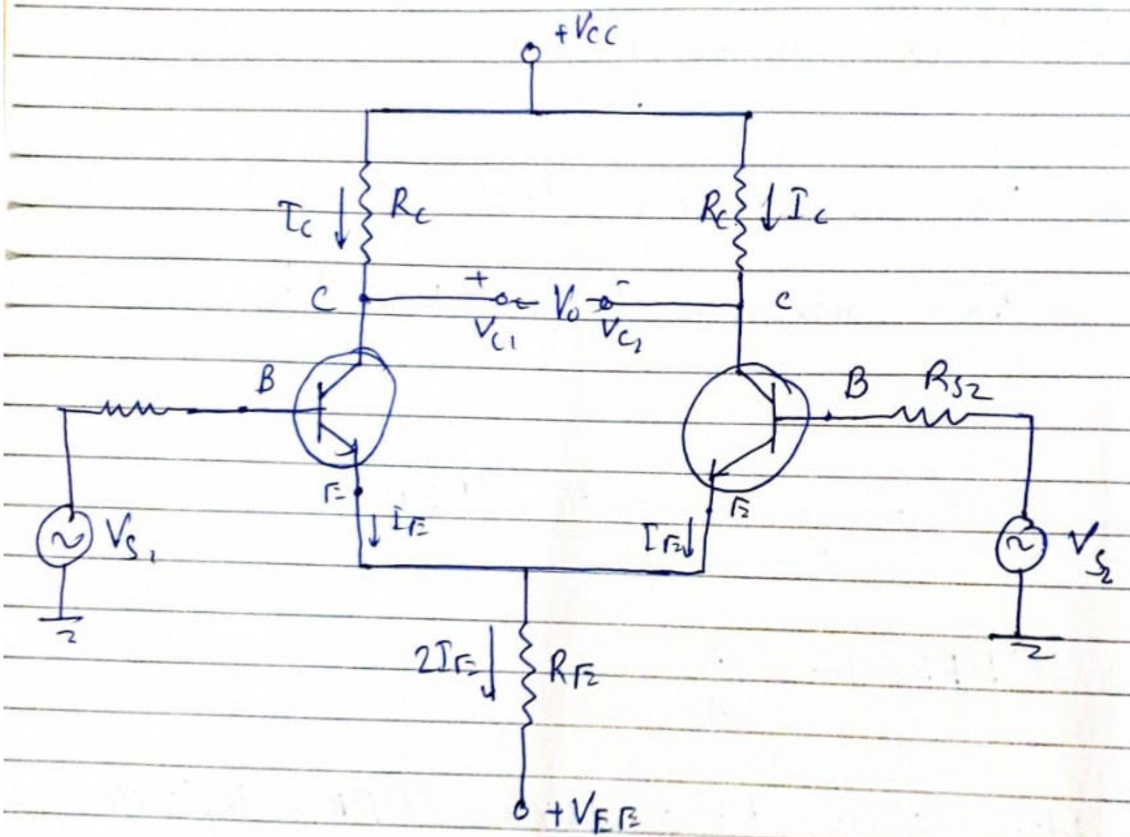
$$CMRR = K_c = \frac{A_d}{A_c}$$

For ideal differential amplifier, CMRR is infinite.

$$A_d = K_c A_c$$

$$\therefore \boxed{V_o = A_d V_d \left[1 + \frac{V_c}{K_c V_d}\right]}$$

Dual i/p, Balanced o/p Differential Amplifier.
(Emitter Coupled Diff. Amplifier)



Emitter coupled differential amplifier

DATE : / /

A dual i/p, balanced o/p differential amp shown in the above figure. It uses two identical transistor connected in CE mode, with emitter coupled together. Hence it is called emitter coupled diff. Amplifier.

V_{CC} & V_{EE} are biasing batteries and R_E is an emitter resistance common to both T_1 & T_2.

Input s/g V_{S_1} & V_{S_2} are applied to the base of Transistor T_1 & T_2 and o/p is collected between their collectors.

Let V_0 be the o/p.

$$V_0 = V_{C_1} - V_{C_2}$$

Analysis

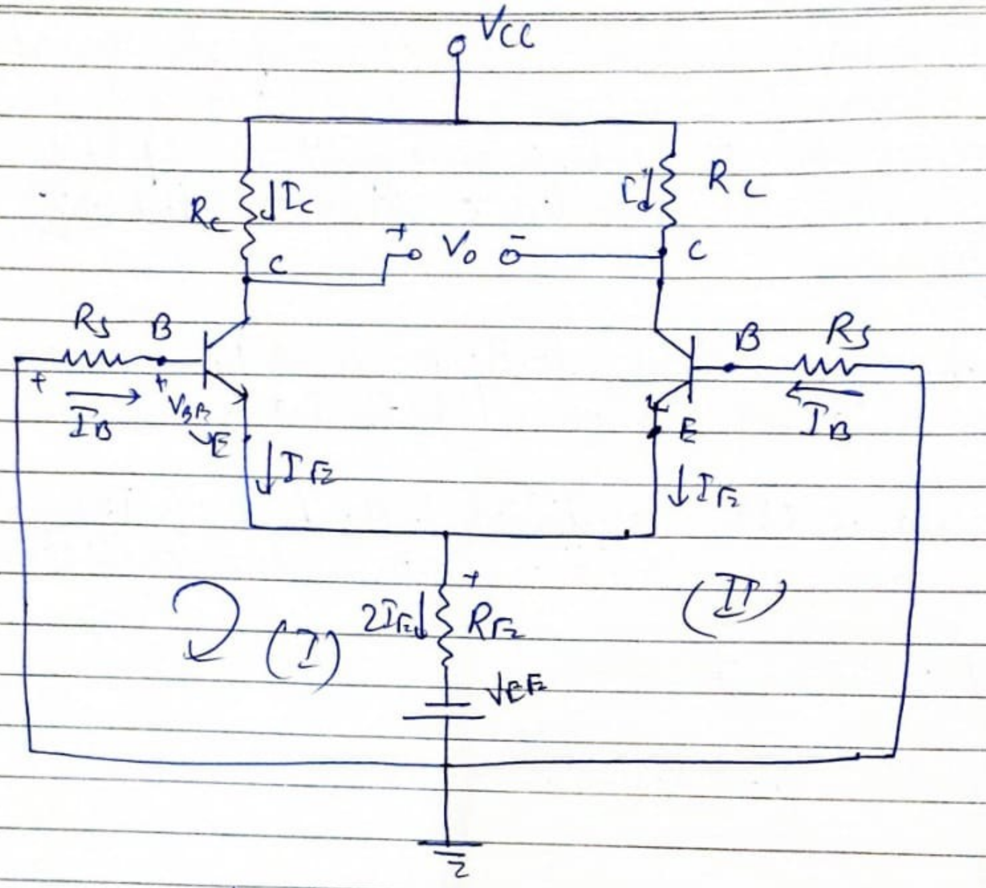
① DC Analysis ② AC Analysis.

Doc Q point V_{CE}, I_C V.G I/p & O/p imp.

DC Analysis

Let us consider the same above ckt of emitter coupled diff. Amp.

The assumption for DC analysis are that AC sources are replaced by short ckt ($V_{S_1} = V_{S_2} = 0$) & let $R_{S_1} = R_{S_2} = R_S$.



Writing mesh equation for loop - 1

$V_{EE} - I_B R_s - V_{BE} - 2 I_E R_E = 0$ —— ①

As we know that

$$I_B = \frac{I_C}{\beta}$$

$I_E = I_C + I_B$

$= I_C + \frac{I_C}{\beta} = I_C\left(\frac{1+\beta}{\beta}\right)$

$\therefore \quad I_E = I_C \left(\frac{1+\beta}{\beta}\right)$

Sub. this values of I_E & I_B in eq ①, we get

$$V_{EE} - \frac{I_C}{\beta} R_s - V_{BE} - \frac{2(1+\beta)}{\beta} I_C R_E = 0$$

$$I_C = \frac{\beta(V_{EE} - V_{BE})}{R_s + 2(1+\beta)R_E}$$

∵ $(1+\beta) \simeq \beta$ & $R_s << 2(1+\beta)R_E$

the above eq. reduces to

$$I_C \cong \frac{\beta(V_{EE} - V_{BE})}{2\beta R_E}$$

$$\boxed{I_C \cong \frac{V_{EE} - V_{BE}}{2R_E}}$$

collector to emitter Voltage (V_{CE})

$$V_{CE} = V_C - V_E \qquad —②$$

$$V_C = V_{CC} - I_E R_E$$

~~no~~ Applying KVL in loop-I along path OBE,

$$-I_b R_s - V_{BE} - V_E = 0$$

$$V_E = -V_{BE} - I_b R_s$$

Since base current I_B is negligible.

$$V_E \cong -V_{BE}$$

Sub. value of V_E & V_C in eq ②

$$V_{CE} = V_{CC} - I_C R_C - (-V_{BE})$$

$$\boxed{V_{CE} = V_{CC} + V_{BE} - I_C R_C} \rightarrow \text{Q point of } T_1$$

Since T_1 & T_2 are identical hence it ~~works~~ has same Q point.

LARGE SIGNAL AMPLIFIERS

Large signal amplifiers also known as power amplifiers are capable of providing large amount of power to the load**.** They are used as last stage in electronic systems. A power amplifier takes the d.c. power supply connected to the output circuit and converts it into a.c. signal power. Output power is controlled by input signal.

Important Features of Power Amplifiers:

- Some of the features of power amplifiers are
- Impedance matching with the load is necessary for delivering max power to the load.
- Power transistors are needed. (To withstand large voltages and currents)
- Power amplifiers are bulk.
- Due to the non–linear characteristics of transistors, Harmonic Distortions are available at the output.

Performance parameters:

The performance of power amplifiers are determined by the following points.

1. **Circuit efficiency:** Also known as conversion efficiency or overall efficiency.

$$\eta = \frac{\text{Max a.c. o/p power}}{\text{d.c. i/p power}}$$

   Its value may be anywhere from 25% to 90%

2. **Distortion:** The difference between the output & input of an amplifier is known as distortion. Even though the output is enlarged and faithful reproduction of input but in actual practice there may be differences in the waveforms or frequencies.

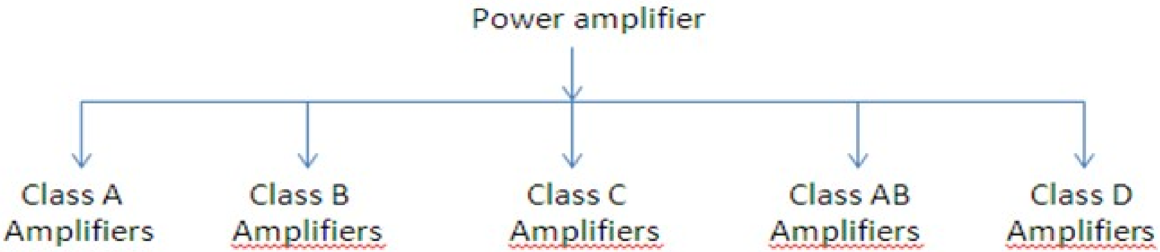
   (1) Harmonic or amplitude distortion – Due to nonlinearity in transistor.

   (2) Crossover distortion – occurs when transistors not operating in correct phase with each other.

3. **Power Dissipation capacity:** It's defined as the ability to dissipate the heat by the power transistor. Also known as power rating. During amplification process large current passes through power transistor hence Heat generated.By connecting a metal sheet (Heat sink) power dissipation capability can be increased.

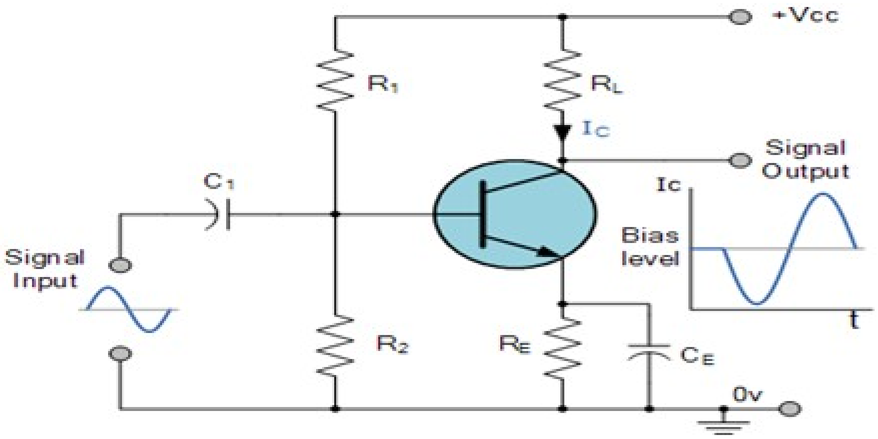
Classification of power amplifiers:

Based on Transistor biasing and amplitude of input signal

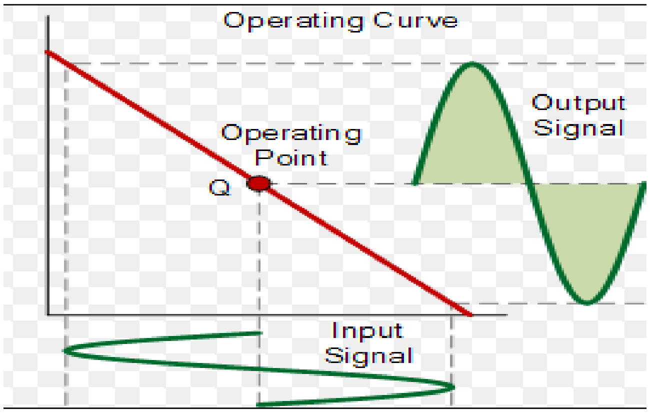


CLASS A POWER AMPLIFIER:

A power amplifier is called Class A amplifier if the transistor used in the circuit conducts for full cycle of the input signal.



The operating point(Q) is selected approximately at the (Biased) centre, so that the output current faithfully follows the input signal. The transistor remains in the **active region** for the full input signal. Transistor is not operated in **Cut off** or **Saturation region**. Transistor conducts for full 360°as shown in Fig .Thus the collector current also flows for full 360° Or full cycle. The base current changes sinusoidally, above and below to the quiescent base current. The collector output current also changes sinusoidally above and below the quiescent current value. They are in phase with each other. Due to this **Ic** change, **Vce** will also change sinusoidally as shown in Fig but out of phase 180. Input is amplified faithfully without any distortions.Since transistor is operatedin active region continuously the collector current and voltage are high.This high collector output produces large power which is dissipated as heat.Hence the efficiency of Class A power amplifier is Low.



Advantages: (1) simple construction

(2) Distortion less output voltage

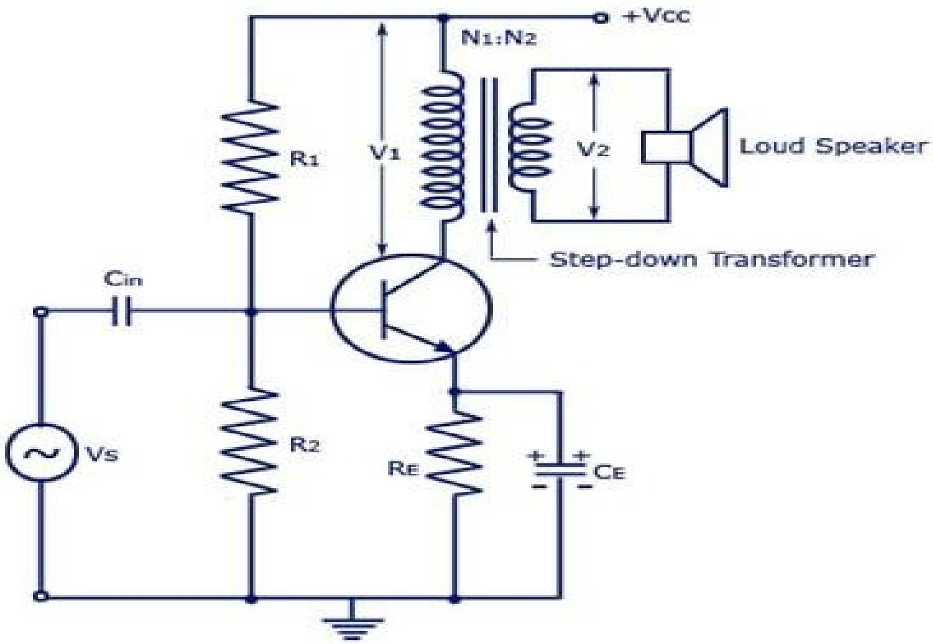
Disadvantage: (1) very low efficiency (25%)

(2) Large power dissipation in the transistors.

(3) Output Impedance is very large.

TRANSFORMER COUPLED CLASS A POWER AMPLIFIER:

Instead of connecting the load directly, the output is connected to the load through a transformer as shown in Fig (4). This set up is used for Impedance matching. This circuit can be useful for low impedance loads like Loudspeakers. By adjusting the turn's ratio (N1\N2) the output impedance is matched with the load impedance.



This type is also known as Single ended Class A amplifier. The primary has negligible d.c. resistance hence no loss of d.c. power. This gives the necessary d.c. isolation to load.

Advantages:

- Max power transfer is done.
- Dc biasing current is doesn't flow through the load so power is saved.
- High efficiency when compared with direct coupled class A amplifier.

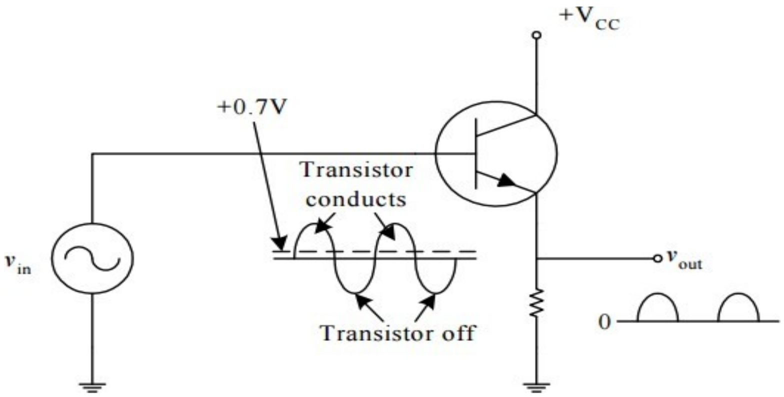
Disadvantage:

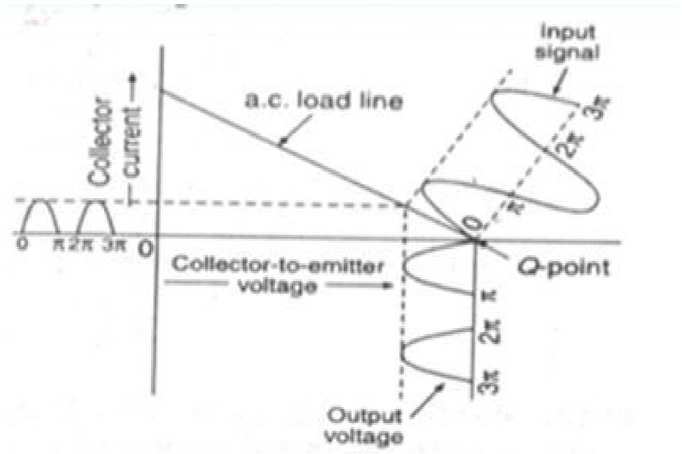
- Circuit design is complicated.
- Circuit is bulky and expensive.
- Due to saturation of transformer core ,secondary induced voltage is zero And

primary current becomes very large.

Class B Power Amplifier:

The output power is obtained for one half cycle of input only. The collector current flows for 180 degrees only. For this the Q point is adjusted so that it is in cut off region





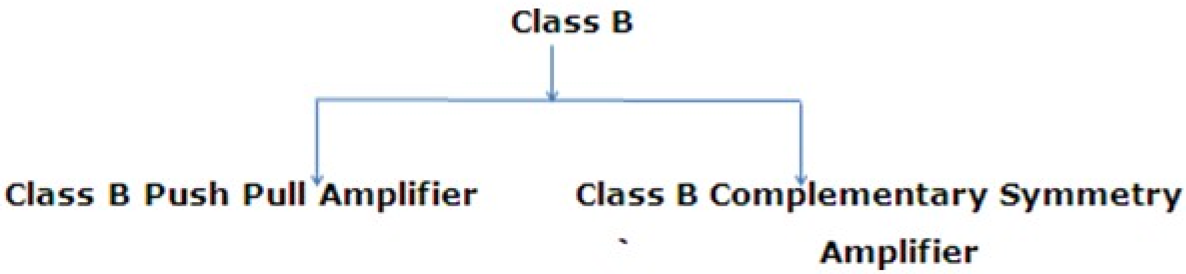
The transistor conducts one half cycle only for the positive half cycle of the input and in Negative cycle of input the transistor goes into Off state. Thus collector current flows only for one half cycle. Since the transistor conducts for one half cycle of the input the power dissipation of these class B amplifiers are very less. Hence efficiency gets increased.

Advantages:

- Impedance with load is possible.
- Second harmonic get automatically cancelled.
- Zero power dissipation.
- High efficiency compared with class A amplifiers.

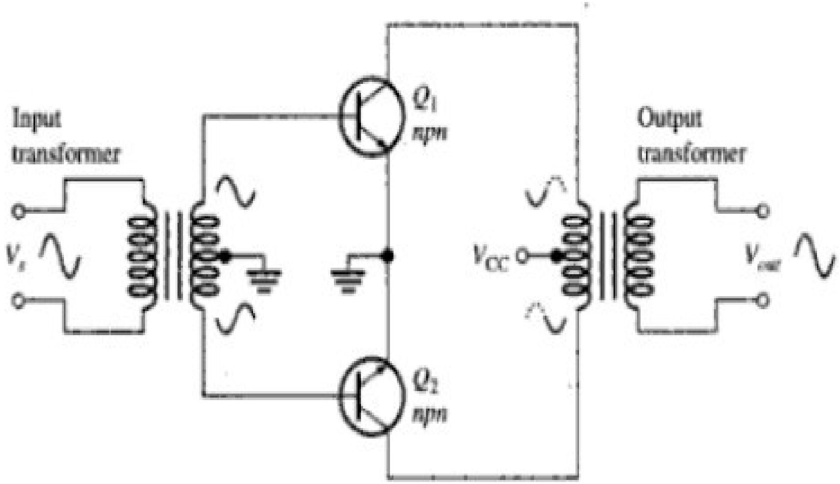
Disadvantage:

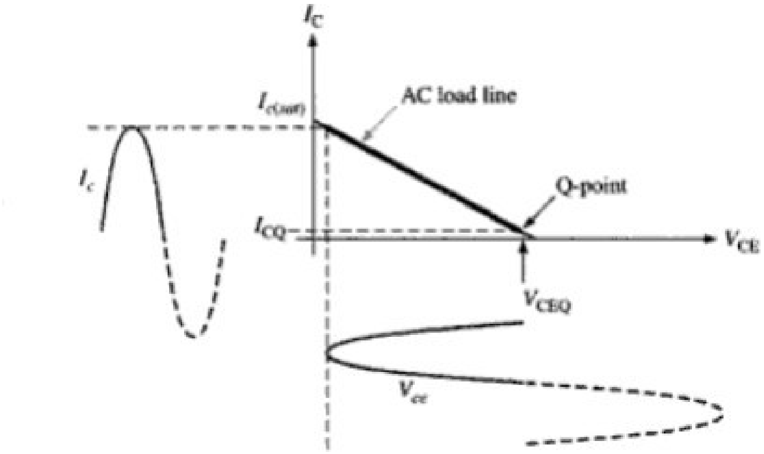
- Crossover distortion is present in the output waveform. Since, the transistor is biased at cut off region the waveform is distorted near zero crossings.
- Efficiency is not so high.



Push Pull Amplifier - If both the transistors are of same type (NPN or PNP) **Complementary Symmetry**- If one of the transistors is NPN & the other one PNP or vice versa.

<u>CLASS B PUSH PULL POWER AMPLIFIER:</u> In class B amplifier output collector current flows only for half cycle for full cycle of the input hence distortion. To get out for full input signal we use Push Pull circuit. Two transformers are used in Push pull amplifiers, one at the input and the other at the load side. Both are centre tapped transformers. As shown in Fig it also contains two transistors Q1 & Q2 both NPN type. Since centre tapped is used Q1 & Q2 are 180 degrees out of phase.(the voltages are equal but with opposite polarity). For positive half cycle Q1(Active region) gives output and Q2 is OFF(cut off region). In negative cycle Q2 is ON & Q1 is OFF. Thus at the output we get a full cycle for a full input signal.





Advantages:

- Efficiency is much higher than class A Amplifier
- Even harmonics get cancelled so harmonic distortion is less.
- Ripples in supply voltage are eliminated

Disadvantage:

- Two centre tapped transformers are necessary
- Hence circuit is bulky and costs more.
- Frequency response is poor.

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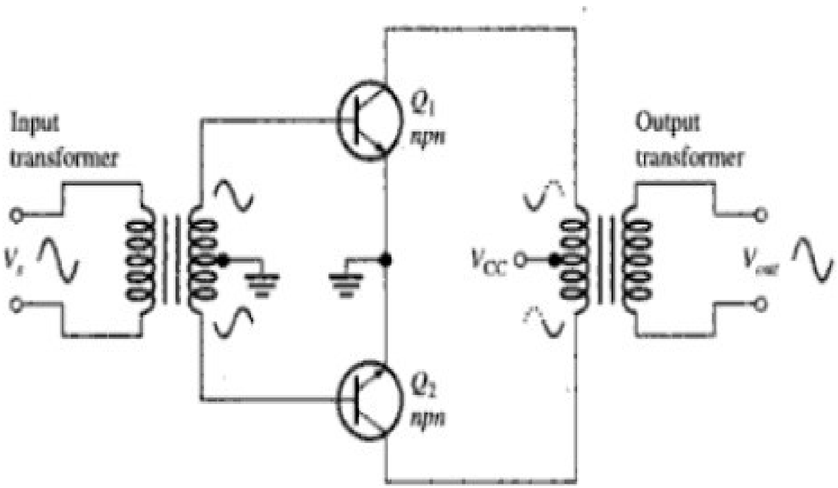

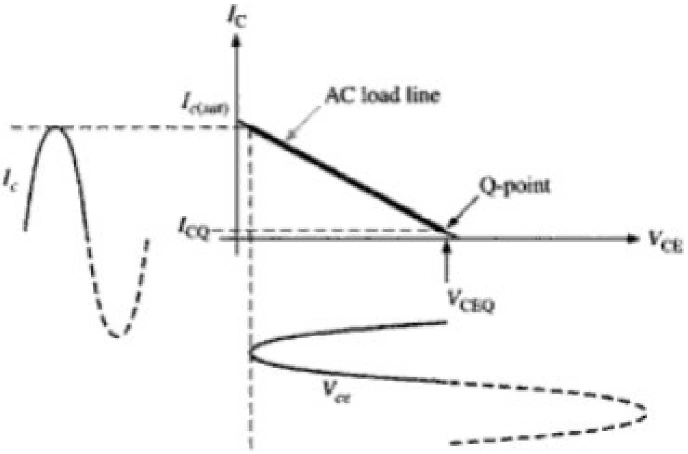

Advantages:

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Disadvantage:

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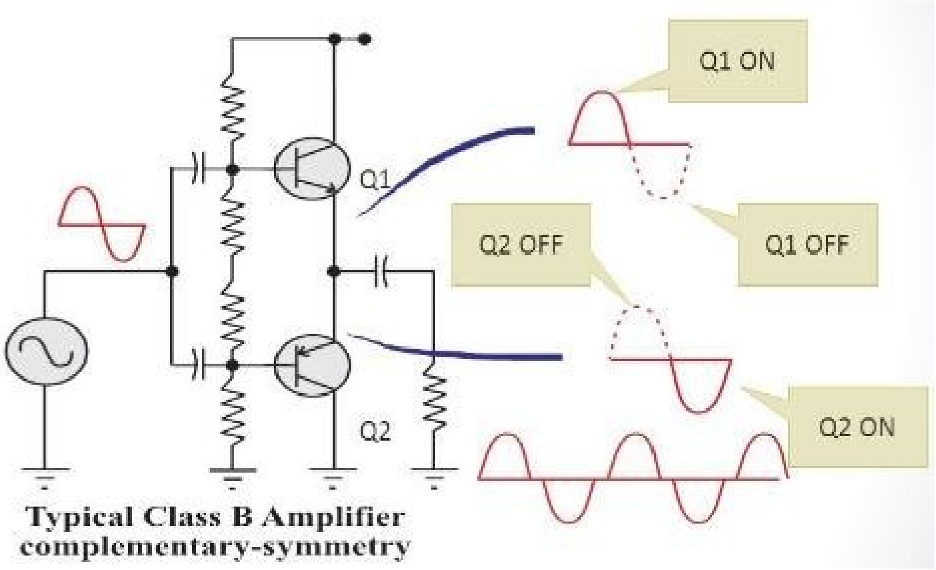
- Hence circuit is bulky and costs more.
- Frequency response is poor.

CLASS B COMPLEMENTARY SYMMETRY AMPLIFIER:

The circuit diagram for complementary symmetry type is shown in Figure(8). This circuit uses two transistors of different type. One is NPN and another PNP. It is a transformer less circuit. For better impedance matching the tow transistors Q1 & Q2 are connected as emitter follower configuration. Positive half cycle Q1 is in Active region so ON & Q2 in cut off So OFF. In negative half cycle Q2 is ON & Q1 is OFF. Thus for a complete input cycle output is developed as shown in figure 8.The difference between complementary symmetry and push pull models is in complementary model there is no output transformer.



Advantages:

- As transformer less circuit the weight and cost is less
- Due to common collector (emitter follower) impedance matching is possible.
- Frequency response is good.
- Value of efficiency is higher than push pull amplifier.

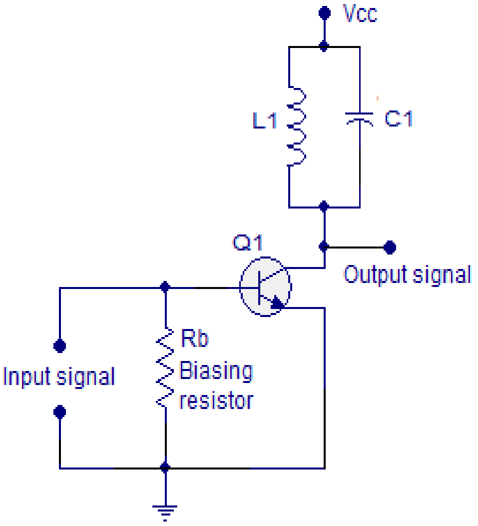
Disadvantage:

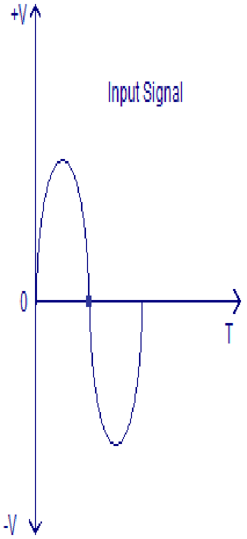
- Circuit needs two separate voltage supplies.
- Output is distorted due to crossover Distortion.
- It is necessary that both transistors Q1 & Q2 have matched characteristics.

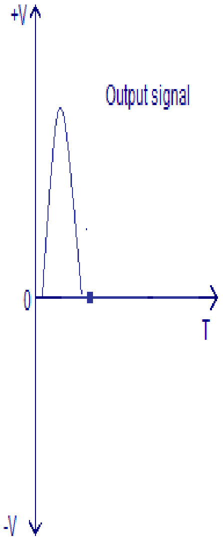
Comparison of Push Pull & Complementary Symmetry circuits:

S No	Parameter	Push Pull	Complementary symmetry
1	Type of Transistor	Both should be of NPN or PNP type	One is PNP and other NPN
2	Use of transformers	Used at both i/p & o/p side	Not needed
3	Impedance matching	Possible due to use of two transformers	Possible due to operation of transistors in CC configuration
4	Transistor Configuration	Both transistors Operates in CE mode	Both transistors Operates in CC mode
5	Conduction Angle	180º	180º
6	Power dissipation when no input is present	Zero	Zero
7	Efficiency	Low	Higher than Push Pull type.

CLASS C AMPLIFIERS:

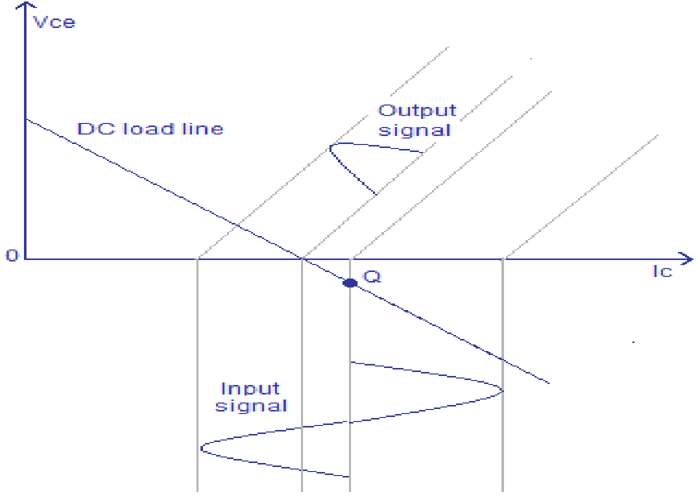






In class C the transistor conducts for less than one half cycle period of the input i.e around 80º to 120º angle. This reduced conduction angle increases the efficiency (Theoretically around 90 %). But this kind of operation causes large distortions. Hence, it is not used in Audio applications. Tuned circuit is used as load as shown in Figure

When the input signal is applied the tuned circuit starts resonating at the frequency of the input signal. Transistor produces a series of current pulses based on the input. By selecting Proper L1, C1 resonance can be achieved. This resonance frequency is extracted by the tuned load at the output.



Advantages:

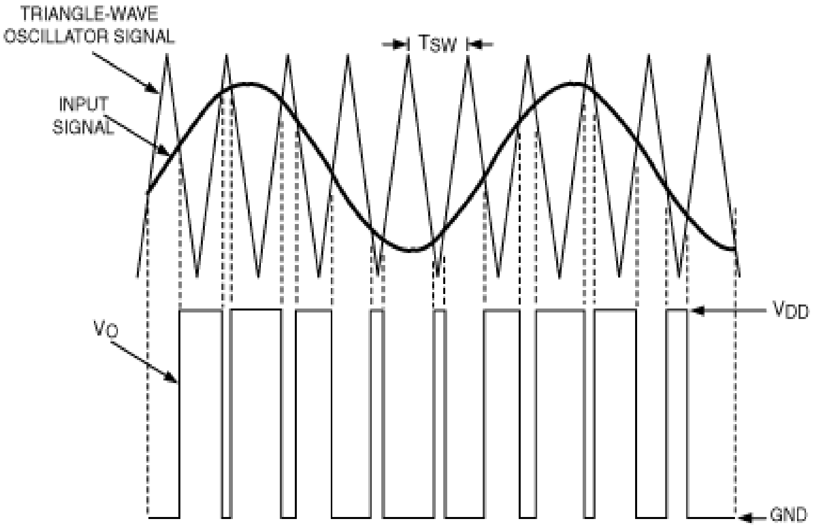
- Less Physical size.
- Used in RF applications.
- High Efficiency (higher than 95%)
- Low power loss in power transistors

Disadvantage:

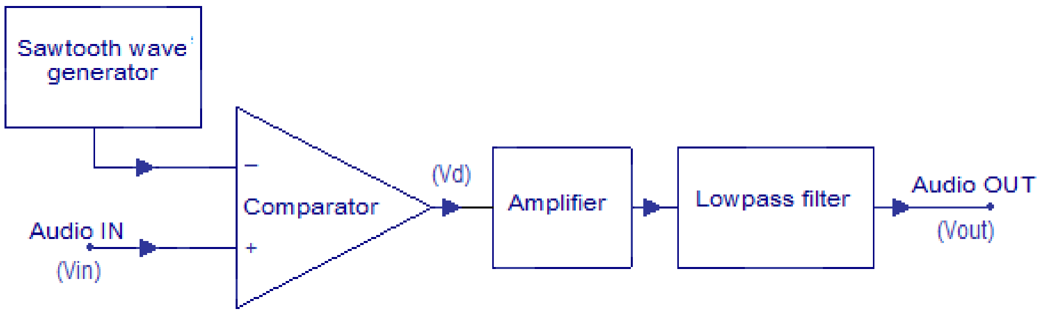
- Creates lot of RF Interference.
- Selection of ideal Inductors is problem.
- Not suitable in Audio applications.

CLASS D AMPLIFIERS:

Class D type is designed to work with pulse or digital input signals. The Input V_{in} is compared with saw tooth wave (known as chopping wave) and accordingly a pulse waveform is generated which is fed to the amplifier.



The circuit diagram of class D amplifier is shown in Figure 12.Input is applied to the non-inverting terminal of the comparator and the saw tooth wave is applied to the inverting terminal. Based on this the comparator produces an output pulse width modulated waveform and this PWM wave is amplified by the amplifier as shown in figure 11. Transistor in the amplifier circuit just acts as a switch and hence the power loss is very less. Low pass filter converts the pulse wave back into sinusoidal signal. At the output thus we have sinusoidal signal.



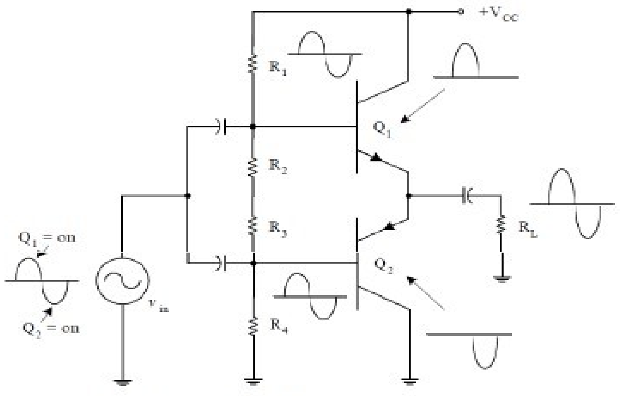
Efficiency: Transistor operates in saturation region when turned on .So V_{ce} is small. This is the reason for class D amplifiers have very high efficiency (Around 90%).

Advantages:

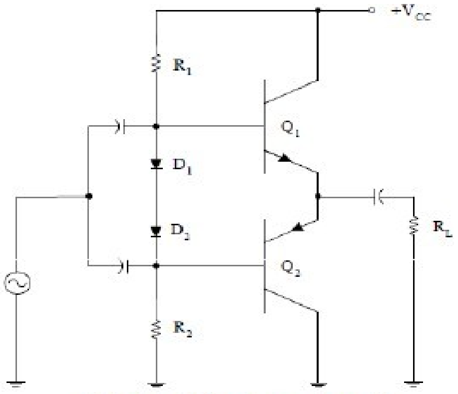
- High efficiency
- Possible to amplify the digital signals and analog signals as well.

CLASS AB AMPLIFIERS:

To eliminate cross over distortion in Class B Push Pull Amplifiers the Biasing of transistors can be done. This arrangement moves the transistor Q point slightly above the cut off region. Usually voltage divider bias is used as shown in Figure13 (a).Due to temperature changes V_{BE} also changes, hence no stable biasing. To avoid this we go for diode biasing as shown in figure 13.b.if D1, D2 matches with the transistor characteristics then we get a stable biasing. The d.c. voltage at the diode is connected to the transistors. (d.c. biasing).This value is equal to cut in voltage, hence conducts for full half cycle of the input. All analysis for class B holds good for class AB power amplifier.



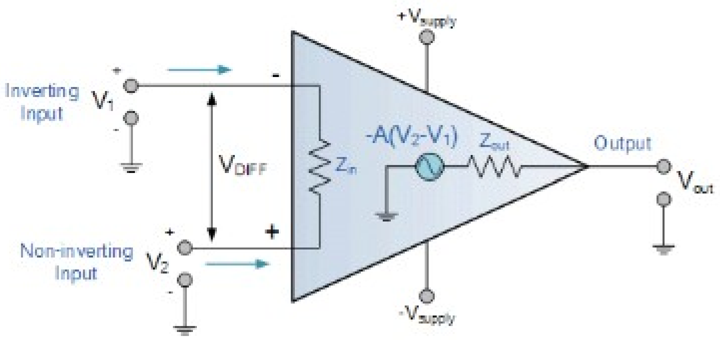
Voltage Divider bias



Diode biasing circuit

Operational Amplifier Basics:

Operational amplifiers are linear devices that have all the properties required for nearly ideal DC amplification and are therefore used extensively in signal conditioning, filtering or to perform mathematical operations such as add, subtract, integration and differentiation.



An **Operational Amplifier**, or op-amp for short, is fundamentally a voltage amplifying device designed to be used with external feedback components such as resistors and capacitors between its output and input terminals. These feedback components determine the resulting function or "operation" of the amplifier and by virtue of the different feedback configurations whether resistive, capacitive or both, the amplifier can perform a variety of different operations, giving rise to its name of "Operational Amplifier".

An *Operational Amplifier* is basically a three-terminal device which consists of two high impedance inputs. One of the inputs is called the **Inverting Input**, marked with a negative or "minus" sign, (–). The other input is called the **Non-inverting Input**, marked with a positive or "plus" sign (+).

A third terminal represents the operational amplifiers output port which can both sink and source either a voltage or a current. In a linear operational amplifier, the output signal is the amplification factor, known as the amplifiers gain (A) multiplied by the value of the input signal and depending on the nature of these input and output signals, there can be four different classifications of operational amplifier gain.

- Voltage – Voltage "in" and Voltage "out"
- Current – Current "in" and Current "out"
- Transconductance – Voltage "in" and Current "out"
- Transresistance – Current "in" and Voltage "out"

Op-amp Parameter and Idealized Characteristic:

Open Loop Voltage Gain(A):

The open loop voltage gain without any feedback for an ideal op amp is infinite. But typical values of open loop voltage gain for a real op amp ranges from 20,000 to 2, 00,000. Let the input voltage be V_{in}. Let A be the open loop voltage gain. Then the output voltage is $V_{out} = AV_{in}$. The value of a typically is in the range specified above but for an ideal op amp, it is infinite.

Input Impedance(Z_{in})

Input Impedance is defined as the input voltage by the input current. The input impedance of an ideal op amp is infinite. That is there no current flowing in the input circuit. However, an ideal op amp has certain current flowing in the input circuit of the magnitude of few pico-amps to a few milli-amps.

Output Impedance (Z_{out})

Output impedance is defined as the ratio of the output voltage to the input current. The output impedance of an ideal op amp is zero, however, real op amps have an output impedance of 10-20 kΩ. An ideal op amp behaves like a perfect voltage source delivering current without any internal losses. The internal resistance reduce the voltage available to the load.

Bandwidth(BW)

An ideal op amp has an infinite bandwidth that is it can amplify any signal from DC to the highest AC frequencies without any losses. So therefore, an ideal op amp is said to have infinite frequency response. In real op amps, the bandwidth is generally limited. The limit depends on the gain bandwidth (GB) product. GB is defined as the frequency where the amplifier gain becomes unity.

Offset Voltage(V_{io})

The offset voltage of an ideal op amp is zero, which means that the output voltage will be zero if the difference between the inverting and non-inverting terminal is zero. If both the terminals are grounded, the output voltage will be zero. But real **op amps** have an offset voltage.

Common Mode Rejection Ratio(CMRR)

Common mode refers to the situation when the same voltage is applied to both the inverting and non-inverting terminal of the op amp. The common mode rejection refers to the ability of the op amp to reject the common mode signal. Now we are in a position to understand the term common mode rejection ratio.

The common mode rejection ratio refers to the measure of the ability of the op amp to reject the common mode signal. Mathematically it is defined as

$$CMRR = |A_D/A_{CM}|$$

Where, A_D is the differential gain of the op amp, ∞ for an ideal op amp.

A_{CM} refers to the common mode gain of the op-amp.

The CMRR of an ideal op amp is ∞. That means it is able to reject all common mode signal. Also from the formula, we can see the A_D is infinite for an ideal op amp and A_{CM} is zero. Therefore the CMRR of an ideal op-amp is infinite.
Therefore it will reject any signal which is common to both. However, real omp have finite CMRR, and does not reject all common mode signals.

Slew Rate:

The slew rate is defined as the maximum rate of output voltage change per unit time. The slew rate helps us to identify the amplitude and maximum input frequency suitable to an operational amplifier (OP amp) such that the output is not significantly distorted. The slew rate should be as high as possible to ensure the maximum undistorted output voltage swing.

Slew rate is a critical factor in ensuring that an OP amp can deliver an output that is reliable to the input. Slew rate changes with the change in voltage gain. Therefore, it is generally specified at unity (+1) gain condition.
A typically general-purpose device may have a slew rate of 10 $V/\mu S$. This means that when a large step input signal is applied to the input, the electronic device can provide an output of 10 volts in 1 microsecond.

Slew Rate Formula

The equation for the slew rate is given by

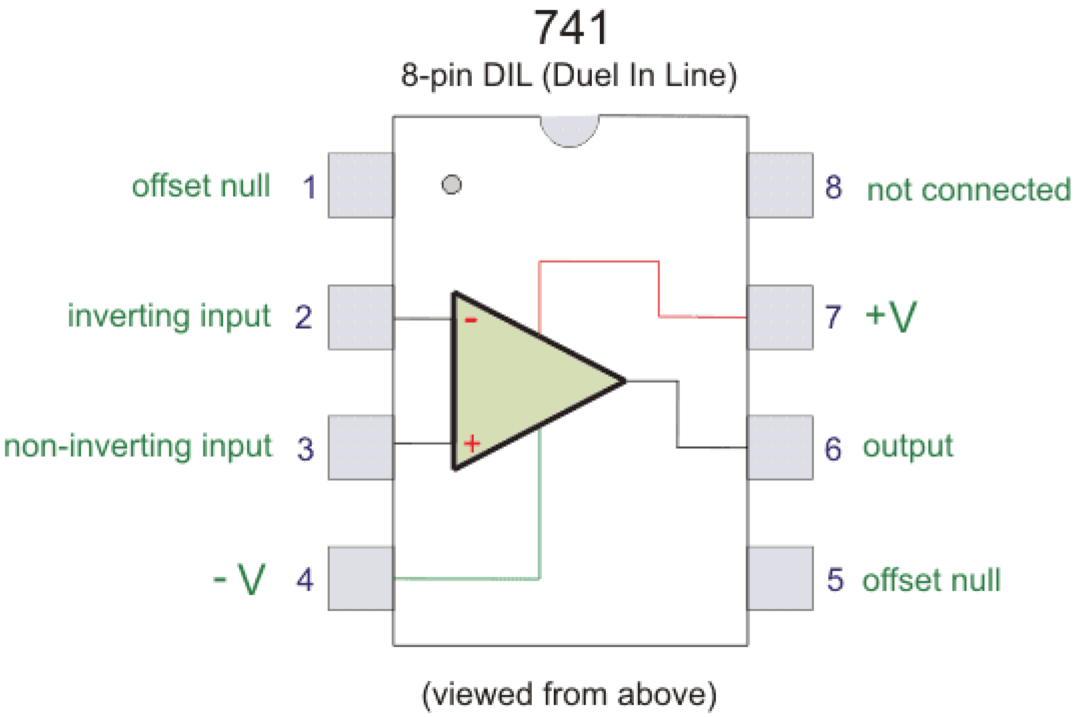
$$S = \frac{dV_0}{dt}|_{maximum}\ Volts/\mu S$$

Slew Rate Units

The unit of slew rate is $Volts/Second$ or $Volts/\mu S$.

Pin Diagram of an Op Amp IC

The op amp IC we are going to discuss about here is IC 741. It is an 8 pin IC. The pin configuration of IC 741 is given below



PIN 1 – Offset Null
PIN 2 – Inverting input

PIN 3 – non- inverting input
PIN 4 – negative voltage supply
PIN 5 – offset null
PIN 6 – output
PIN 7 – positive voltage supply
PIN 8 – not connected