JAIPUR ENGINEERING COLLEGE AND RESEARCH CENTRE

Jaipur Engineering College & Research Centre, Jaipur

Lecture Notes

3EE4-06: Analog Electronics

ACADEMIC SESSION 2020-21

Prepared By:
Jisha Varghese

VISION OF ELECTRICAL ENGINEERING DEPARTMENT

Electrical Engineering Department strives to be recognized globally for outcome based knowledge and to develop human potential to practice advance technology which contribute to society.

MISSION OF ELECTRICAL ENGINEERING DEPARTMENT

M1. To impart quality technical knowledge to the learners to make them globally competitive Electrical Engineers.

M2. To provide the learners ethical guidelines along with excellent academic environment for a long productive career.

M3. To promote industry-institute relationship.

PROGRAM OUTCOMES

1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems in Electrical Engineering.
2. **Problem analysis:** Identify, formulate, research literature, and analyze complex engineering problems reaching substantial conclusions using first principles of mathematics, natural sciences, and engineering sciences in Electrical Engineering.
3. **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations using Electrical Engineering.
4. **Conduct investigations of complex problems:** Use research based knowledge and research methods including design of experiments, analysis and interpretation of data and synthesis of the information to provide valid conclusions using Electrical Engineering.
5. **Modern tool usage:** Create, select and apply appropriate techniques, resources, and modern engineering and EE tools including prediction and modeling to complex engineering activities with an understanding of the limitations in EE.
6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice using EE.
7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of EE and need for sustainable development in EE.
8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice using EE.
9. **Individual and team work:** Function effectively as an individual and as a member or leader in diverse teams, and multi-disciplinary settings in EE.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations and give and receive clear instructions.
11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage EE projects and in multi-disciplinary environments.
12. **Life-long learning:** Recognize the need for and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological changes needed in EE.

COURSE OUTCOMES:

On successful completion of the course, the students will be able to: -

CO 1	Understand the characteristics of Diodes, concepts behind the Clippers, and Clampers. Design and analysis of various rectifier and amplifier circuits
CO 2	Analyze the characteristics of current flow in a bipolar junction transistor and MOSFET & different electronic devices such as Amplifiers
CO 3	Understand the dynamics of Linear & Non Linear Devices

Syllabus

RAJASTHAN TECHNICAL UNIVERSITY, KOTA

SYLLABUS

2nd Year - III Semester: B.Tech. (Electrical Engineering)

3EE4-06: Analog Electronics

Credit: 3
3L+0T+0P

Max. Marks: 150 (IA:30, ETE:120)
End Term Exam: 3 Hours

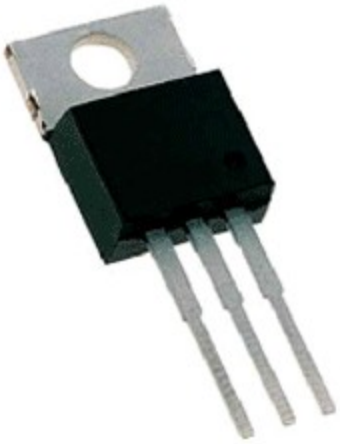
SN		Hours
1.	**Diode circuits** P-N junction diode, I-V characteristics of a diode; review of half-wave and full-wave rectifiers, Zener diodes, clamping and clipping circuits.	4
2.	**BJT circuits** Structure and I-V characteristics of a BJT; BJT as a switch. BJT as an amplifier: small-signal model, biasing circuits, current mirror; common-emitter, common-base and common collector amplifiers; Small signal equivalent circuits, high-frequency equivalent circuits.	8
3.	**MOSFET circuits** MOSFET structure and I-V characteristics. MOSFET as a switch. MOSFET as an amplifier: small-signal model and biasing circuits, common-source, common-gate and common-drain amplifiers; small signal equivalent circuits - gain, input and output impedances, transconductance, high frequency equivalent circuit.	8
4.	**Differential, multi-stage and operational amplifiers** Differential amplifier; power amplifier; direct coupled multi-stage amplifier; internal structure of an operational amplifier, ideal op-amp, non-idealities in an op-amp (Output offset voltage, input bias current, input offset current, slew rate, gain bandwidth product)	8
5.	**Linear applications of op-amp** Idealized analysis of op-amp circuits. Inverting and non-inverting amplifier, differential amplifier, instrumentation amplifier, integrator, active filter, P, PI and PID controllers and lead/lag compensator using an op-amp, voltage regulator, oscillators (Wein bridge and phase shift). Analog to Digital Conversion.	8
6.	**Nonlinear applications of op-amp** Hysteretic Comparator, Zero Crossing Detector, Square-wave and triangular-wave generators, Precision rectifier, peak detector. Monoshot	6
	TOTAL	42

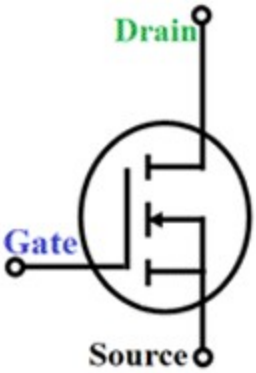
Office of Dean Academic Affairs
Rajasthan Technical University, Kota

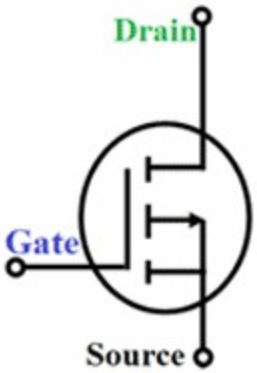
Unit: 3

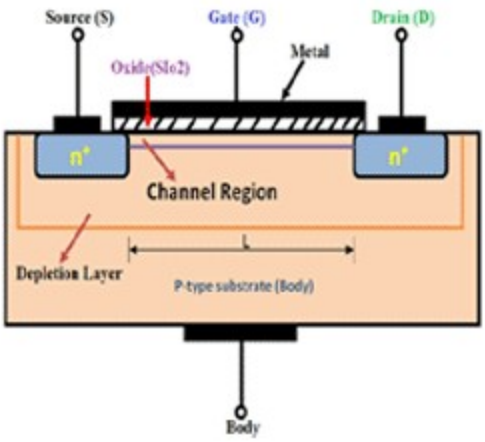
Chapter: MOSFET CIRCUIT

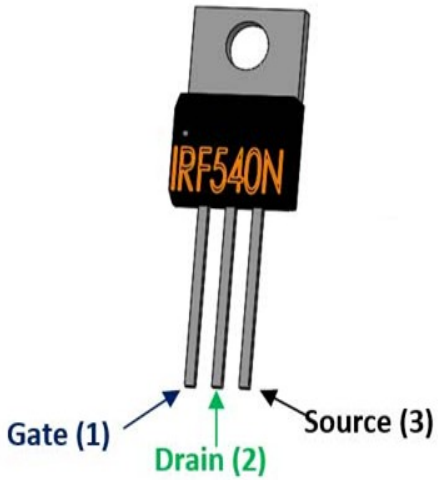
MOSFETs are tri-terminal, unipolar, voltage-controlled, high input impedance devices which form an integral part of vast variety of electronic circuits. These devices can be classified into two types viz., depletion-type and enhancement-type, depending on whether they possess a channel in their default state or no, respectively. Further, each of them can be either p-channel or n-channel devices as they can have their conduction current due to holes or electrons respectively.











In general, any MOSFET is seen to exhibit three operating regions viz.,

1. Cut-Off Region

Cut-off region is a region in which the MOSFET will be OFF as there will be no current flow through it. In this region, MOSFET behaves like an open switch and is thus used when they are required to function as electronic switches.

2. Ohmic or Linear Region

Ohmic or linear region is a region where in the current I_{DS} increases with an increase in the value of V_{DS}. When MOSFETs are made to operate in this region, they can be used as amplifiers.

3. Saturation Region

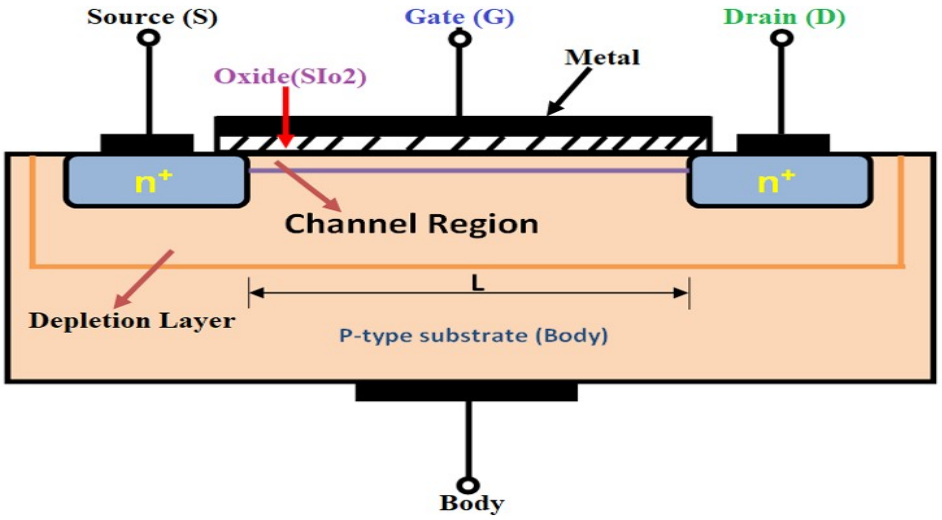
In saturation region, the MOSFETs have their I_{DS} constant inspite of an increase in V_{DS} and occurs once V_{DS} exceeds the value of pinch-off voltage V_P. Under this condition, the device will act like a closed switch through which a saturated value of I_{DS} flows. As a result, this operating region is chosen whenever MOSFETs are required to perform switching operations.

Types of MOSFET

1. Depletion type MOSFET
2. Enhancement type MOSFET

Construction Of MOSFET

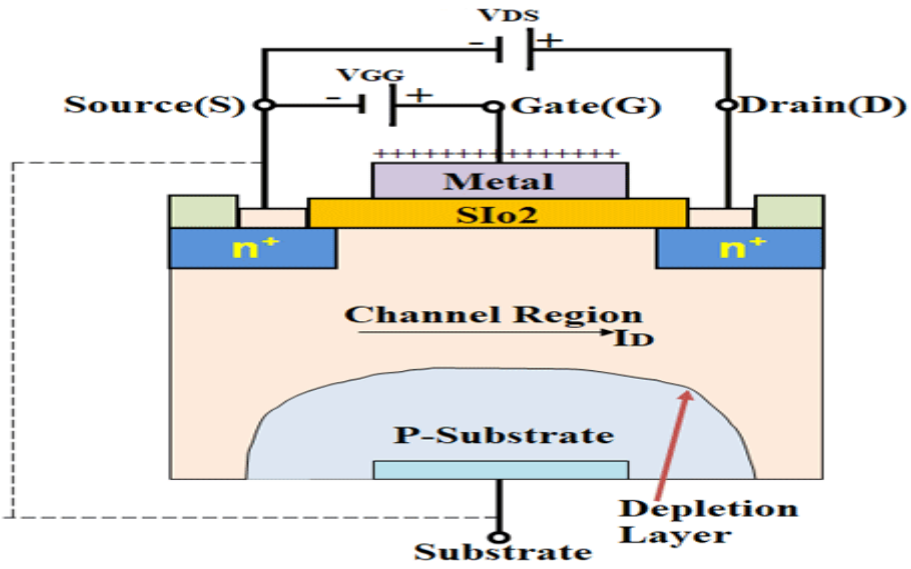
The below image shows the typical **internal structure of the MOSFET**. Although the MOSFET is an advanced form of FET and operates with the same three terminals as a FET the internal structure of the MOSFET is really different from the general FET.



The gate terminal is fixed on the thin metal layer which is insulated by a layer of Silicon Dioxide (SiO2) from the semiconductor, and you will be able to see two N-type semiconductors fixed in the channel region where the drain and source terminals are placed. The channel between the drain and source of the MOSFET is an N-type, opposite to this, the substrate is implemented as P-type. This helps in biasing MOSFET in both the polarities, either positive or negative. If the gate terminal of the MOSFET isn't biased, it will stay in the non-conductive state, hence the MOSFET is mostly used in designing switches and logic gates.

Working Principle of MOSFET

In general, the MOSFET works as a switch, the MOSFET controls the voltage and current flow between the source and drain. The **working of the MOSFET** depends on the **MOS capacitor**, which is the semiconductor surface below the oxide layers between the source and drain terminal. It can be inverted from p-type to n-type, simply by applying positive or negative gate voltage respectively. The below image shows the block diagram of the MOSFET.



When a **drain-source voltage (V_{DS})** is connected between the drain and source, a positive voltage is applied to the Drain, and the negative voltage is applied to the Source. Here the PN junction at the drain is reverse biased and the PN junction at the Source is forward biased. At this stage, there will not be any current flow between the drain and the source.

If we apply a positive voltage (V_{GG}) to the gate terminal, due to electrostatic attraction the minority charge carriers (electrons) in the P substrate will start to accumulate on the gate contact which forms a conductive bridge between the two n+ regions. The number of free electrons accumulated at the gate contact depends on the strength of positive voltage applied. The higher

the applied voltage greater the width of the n-channel formed due to electron accumulation, this eventually increases the conductivity and the **drain current (I_D)** will start to flow between the Source and Drain.

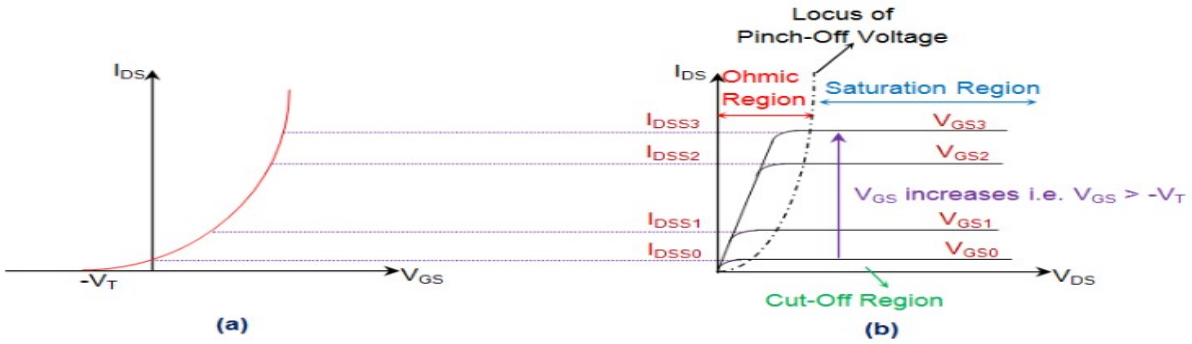
When there is no voltage applied to the gate terminal, there will not be any current flow apart from a small amount of current due to minority charge carriers. The minimum voltage at which the MOSFET starts conducting is called the **threshold voltage**.

Operation of MOSFET in Depletion Mode:

The depletion-mode MOSFETs are usually called the "Switched ON" devices as they are generally in the closed state when there is no bias voltage at the gate terminal. When we increase the applied voltage to the gate in positive the channel width will be increased in depletion mode. This will increase the drain current I_D through the channel. If the applied gate voltage is highly negative, then the channel width will be less and the MOSFET might enter into the cutoff region.

VI characteristics:

The **V-I characteristics of the depletion-mode MOSFET** transistor are drawn between the drain-source voltage (V_{DS}) and Drain current (I_D). The small amount of voltage at the gate terminal will control the current flow through the channel. The channel formed between the drain and the source will act as a good conductor with zero bias voltage at the gate terminal. The channel width and drain current will increase if the positive voltage is applied to the gate whereas they will get decreased when we apply a negative voltage to the gate.



***n*-Channel Depletion type MOSFET (a) Transfer Characteristics (b) Output Characteristics**

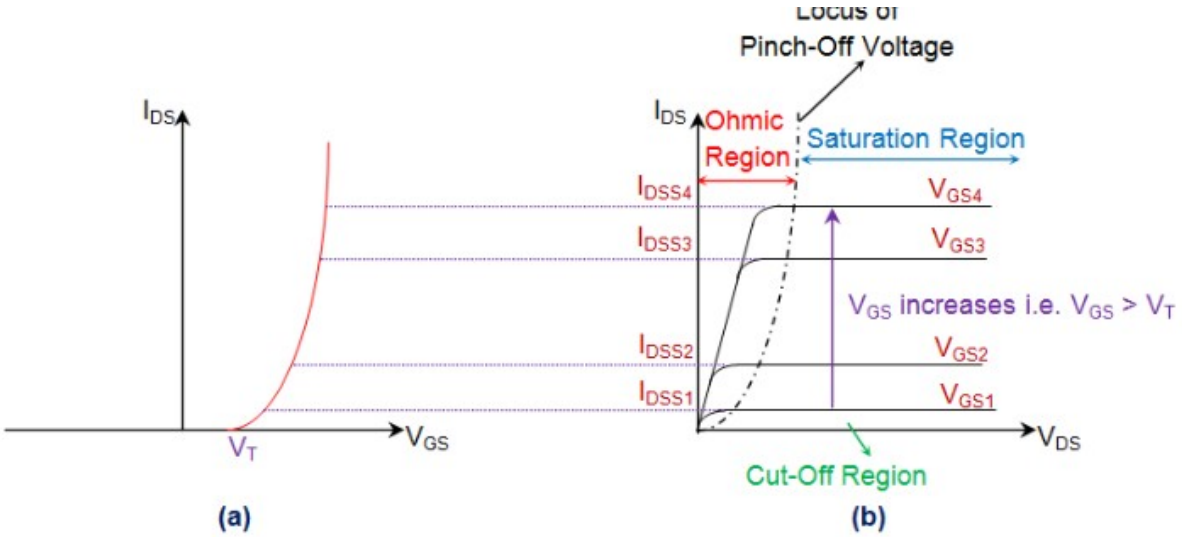
Operation of MOSFET in Enhancement Mode:

The operation of MOSFET in Enhancement mode is similar to the operation of the open switch, it will start to conduct only if the positive voltage($+V_{GS}$) is applied to the gate terminal and the drain current starts to flow through the device. The channel width and drain current will increase

when the bias voltage increases. But if the applied bias voltage is zero or negative the transistor will remain in the OFF state itself.

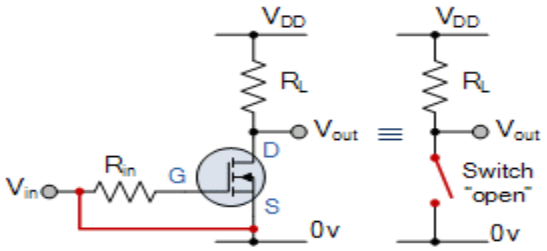
VI Characteristics:

VI characteristics of the enhancement-mode MOSFET are drawn between the drain current (I_D) and the drain-source voltage (V_{DS}). The VI characteristics are partitioned into three different regions, namely ohmic, saturation, and cut-off regions. The cutoff region is the region where the MOSFET will be in the OFF state where the applied bias voltage is zero. When the bias voltage is applied, the MOSFET slowly moves towards conduction mode, and the slow increase in conductivity takes place in the ohmic region. Finally, the saturation region is where the positive voltage is applied constantly and the MOSFET will be staying in the conduction state.



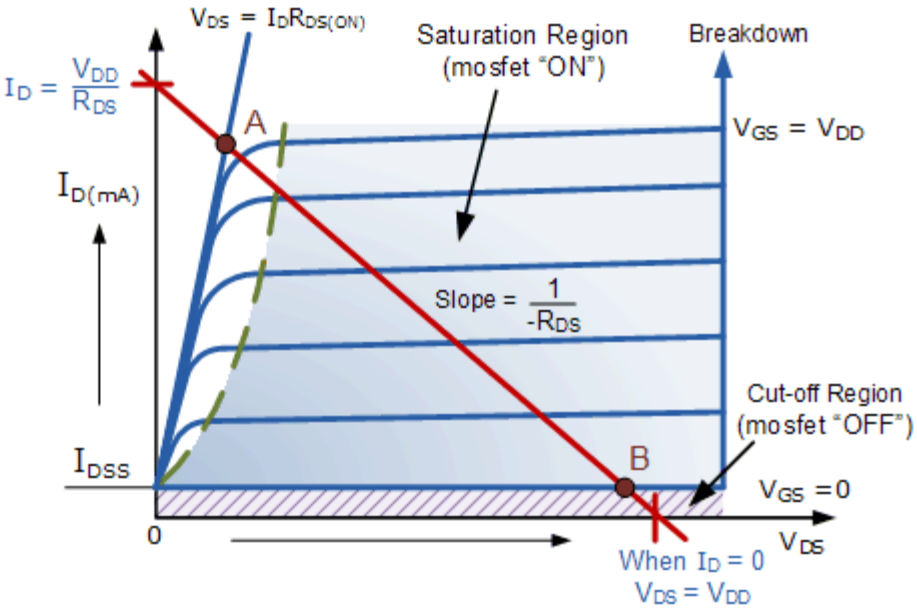
***n*-Channel Enhancement type MOSFET (a) Transfer Characteristics (b) Output Characteristics**

MOSFET as a switch:



MOSFET's make very good electronic switches for controlling loads and in CMOS digital circuits as they operate between their cut-off and saturation regions.

MOSFET Characteristics Curves



The minimum ON-state gate voltage required to ensure that the MOSFET remains "ON" when carrying the selected drain current can be determined from the V-I transfer curves above. When V_{IN} is HIGH or equal to V_{DD}, the MOSFET Q-point moves to point A along the load line.

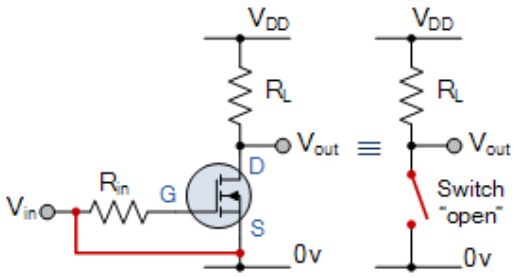
The drain current I_D increases to its maximum value due to a reduction in the channel resistance. I_D becomes a constant value independent of V_{DD}, and is dependent only on V_{GS}. Therefore, the transistor behaves like a closed switch but the channel ON-resistance does not reduce fully to zero due to its $R_{DS(on)}$ value, but gets very small.

Likewise, when V_{IN} is LOW or reduced to zero, the MOSFET Q-point moves from point A to point B along the load line. The channel resistance is very high so the transistor acts like an open circuit and no current flows through the channel. So if the gate voltage of the MOSFET toggles between two values, HIGH and LOW the MOSFET will behave as a "single-pole single-throw" (SPST) solid state switch and this action is defined as:

1. Cut-off Region

Here the operating conditions of the transistor are zero input gate voltage (V_{IN}), zero drain current I_D and output voltage $V_{DS} = V_{DD}$. Therefore for an enhancement type MOSFET the conductive channel is closed and the device is switched "OFF".

Cut-off Characteristics



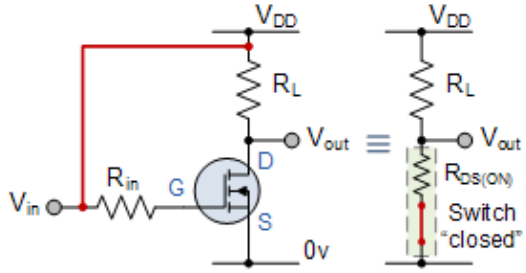
- The input and Gate are grounded (0V)
- Gate-source voltage less than threshold voltage $V_{GS} < V_{TH}$
- MOSFET is "OFF" (Cut-off region)
- No Drain current flows ($I_D = 0$ Amps)
- $V_{OUT} = V_{DS} = V_{DD} = "1"$
- MOSFET operates as an "open switch"

Then we can define the cut-off region or "OFF mode" when using an e-MOSFET as a switch as being, gate voltage, $V_{GS} < V_{TH}$ thus $I_D = 0$. For a P-channel enhancement MOSFET, the Gate potential must be more positive with respect to the Source.

2. Saturation Region

In the saturation or linear region, the transistor will be biased so that the maximum amount of gate voltage is applied to the device which results in the channel resistance $R_{DS(on)}$ being as small as possible with maximum drain current flowing through the MOSFET switch. Therefore for the enhancement type MOSFET the conductive channel is open and the device is switched "ON".

Saturation Characteristics



- The input and Gate are connected to V_{DD}
- Gate-source voltage is much greater than threshold voltage $V_{GS} > V_{TH}$
- MOSFET is "ON" (saturation region)
- Max Drain current flows ($I_D = V_{DD} / R_L$)
- $V_{DS} = 0V$ (ideal saturation)
- Min channel resistance $R_{DS(on)} < 0.1\Omega$
- $V_{OUT} = V_{DS} \cong 0.2V$ due to $R_{DS(on)}$
- MOSFET operates as a low resistance "closed switch"

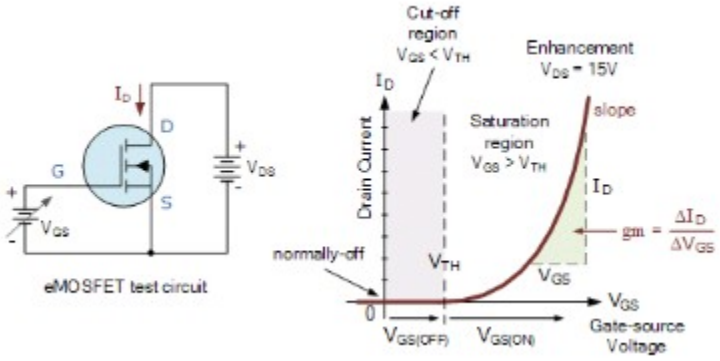
Then we can define the saturation region or "ON mode" when using an e-MOSFET as a switch as gate-source voltage, $V_{GS} > V_{TH}$ thus I_D = Maximum. For a P-channel enhancement MOSFET, the Gate potential must be more negative with respect to the Source.

By applying a suitable drive voltage to the gate of an FET, the resistance of the drain-source channel, $R_{DS(on)}$ can be varied from an "OFF-resistance" of many hundreds of kΩ, effectively an open circuit, to an "ON-resistance" of less than 1Ω, effectively acting as a short circuit.

When using the MOSFET as a switch we can drive the MOSFET to turn "ON" faster or slower, or pass high or low currents. This ability to turn the power MOSFET "ON" and "OFF" allows the device to be used as a very efficient switch with switching speeds much faster than standard bipolar junction transistors.

MOSFET Amplifier:

MOSFET Amplifier uses a metal-oxide silicon transistor connected in the common source configuration.



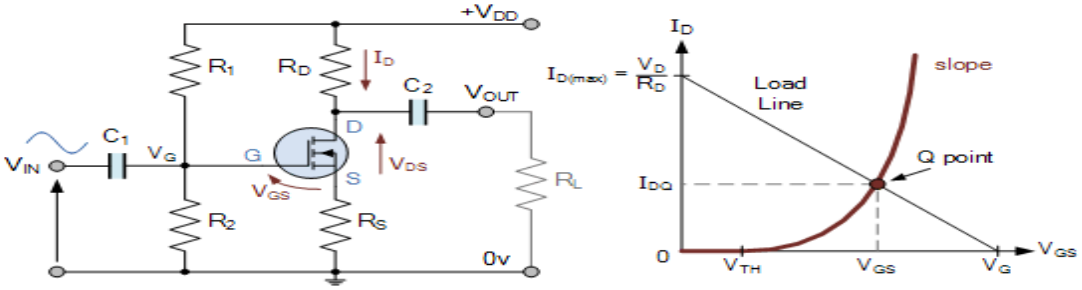
Enhancement MOSFET Amplifier

Enhancement MOSFET, or eMOSFET, can be classed as normally-off (non-conducting) devices, that is they only conduct when a suitable gate-to-source positive voltage is applied, unlike Depletion type mosfets which are normally-on devices conducting when the gate voltage is zero.

However, due to the construction and physics of an enhancement type mosfet, there is a minimum gate-to-source voltage, called the threshold voltage V_{TH} that must be applied to the gate before it starts to conduct allowing drain current to flow. In other words, an enhancement mosfet does not conduct when the gate-source voltage, V_{GS} is less than the threshold voltage, V_{TH} but as the gates forward bias increases, the drain current, I_D (also known as drain-source current I_{DS}) will also increase, similar to a bipolar transistor, making the eMOSFET ideal for use in mosfet amplifier circuits.

The characteristics of the MOS conductive channel can be thought of as a variable resistor that is controlled by the gate. The amount of drain current that flows through this n-channel therefore depends on the gate-source voltage and one of the many measurements we can take using a mosfet is to plot a transfer characteristics graph to show the i-v relationship between the drain current and the gate voltage as shown.

Basic MOSFET Amplifier



This simple enhancement-mode common source mosfet amplifier configuration uses a single supply at the drain and generates the required gate voltage, V_G using a resistor divider. We remember that for a MOSFET, no current flows into the gate terminal and from this we can make the following basic assumptions about the MOSFET amplifiers DC operating conditions.

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$
$$= I_D (R_D + R_S) + V_{DS}$$

$$\therefore R_D + R_S = \frac{V_{DD} - V_{DS}}{I_D}$$

$$V_{GS} = V_G - I_S R_S$$

for proper operation of the mosfet, this gate-source voltage must be greater than the threshold voltage of the mosfet, that is $V_{GS} > V_{TH}$. Since $I_S = I_D$, the gate voltage, V_G is therefore equal too

$$V_{GS} = V_G - I_D R_S$$

$$\therefore V_G = V_{GS} + I_D R_S$$

$$\text{or } V_G = V_{GS} + V_S$$

To set the mosfet amplifier gate voltage to this value we select the values of the resistors, R1 and R2 within the voltage divider network to the correct values. As we know from

above, “no current” flows into the gate terminal of a mosfet device so the formula for voltage division is given as:

Small Signal Model

In the **small-signal** analysis, one assumes that the device is biased at a DC operating point (also called the Q point or the quiescent point), and then, a **small signal** is super-imposed on the DC biasing point.
Small Signal Analysis of JFET and MOSFET Amplifiers BIASING OF FET AMPLIFIERS Fixed Bias Unlike BJTs, thermal runaway does not occur with FETs. However, the wide differences in maximum and minimum transfer characteristics make ID levels unpredictable with simple fixed-gate bias voltage. To obtain reasonable limits on quiescent drain currents ID and drain-source voltage VDS, source resistor and potential divider bias techniques must be used. With few exceptions, MOSFET bias circuits are similar to those used for JFETs. Various FET biasing circuits are discussed below: Fixed Bias:

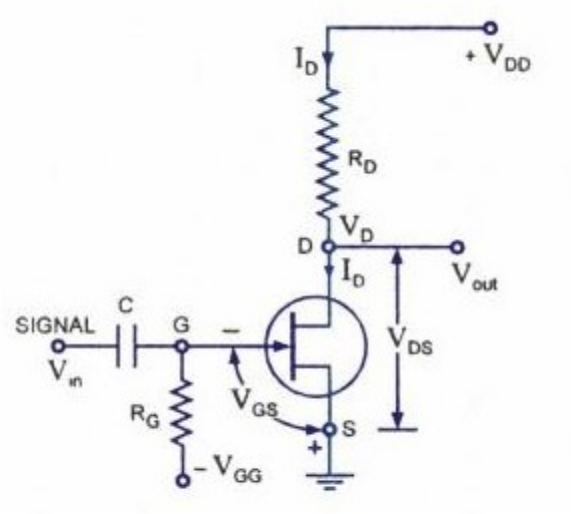


FIG.: Fixed biasing circuit for JFET

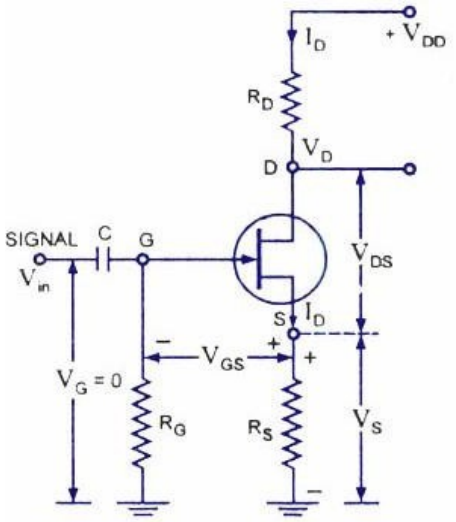
DC bias of a FET device needs setting of gate-source voltage V_{GS} to give desired drain current I_D . For a JFET drain current is limited by the saturation current I_{DS}. Since the FET has such a high input impedance that no gate current flows and the dc voltage of the gate set by a voltage divider or a fixed battery voltage is not affected or loaded by the FET.
Fixed dc bias is obtained using a battery V_{QG}. This battery ensures that the gate is always negative with respect to source and no current flows through resistor R_G and gate terminal that is I_G =0. The battery provides a voltage V_{GS} to bias the N-channel JFET, but no resulting current is drawn from the battery V_{GG}. Resistor R_G is included to allow any ac signal applied through capacitor C to develop across R_G. While any ac signal will develop across R_G, the dc voltage drop across R_G is equal to $I_G R_G$ = 0 volt.

The gate-source voltage V_{GS} is then $V_{GS} = - v_G - v_s = - v_{GG} - 0 = - V_{GG}$

The drain to source current I_D is then fixed by the gate-source voltage as determined by equation.

This current then causes a voltage drop across the drain resistor R_D and is given as $V_{RD} = I_D R_D$ and output voltage, $V_{out} = V_{DD} - I_D R_D$

Self bias:



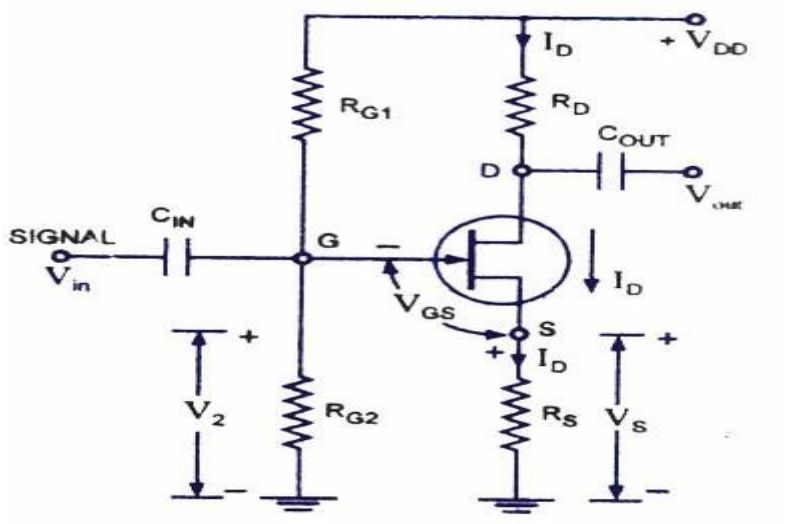
This is the most common method for biasing a JFET. Self-bias circuit for N-channel JFET is shown in figure. Since no gate current flows through the reverse-biased gate-source, the gate current $I_G = 0$ and, therefore,$v_G = i_G R_G = 0$ With a drain current I_D the voltage at the S is, $V_s = I_D R_s$. The gate-source voltage is then,

$V_{Gs} = V_G - V_s = 0 - I_D R_s = - I_D R_s$. So, voltage drop across resistance R_s provides the biasing voltage V_{Gg} and no external source is required for biasing and this is the reason that it is called self-biasing. The operating point *(*that is zero signal I_D and V_{DS}) can easily be determined from equation and equation given below :

$V_{DS} = V_{DD} - I_D (R_D + R_S)$

Thus dc conditions of JFET amplifier are fully specified. Self biasing of a JFET stabilizes its quiescent operating point against any change in its parameters like transconductance. Let the given JFET be replaced by another JFET having the double conductance then drain current will also try to be double but since any increase in voltage drop across R_s, therefore, gate-source voltage, V_{GS} becomes more negative and thus increase in drain current is reduced.

Potential Divider Bias for JFET:



A slightly modified form of dc bias is provided by the circuit shown in figure. The resistors R_{Gl} and R_{G2} form a potential divider across drain supply V_{DD}. The voltage V_2 across R_{G2} provides the necessary bias. The additional gate resistor R_{Gl} from gate to supply voltage facilitates in larger adjustment of the dc bias point and permits use of larger valued R_S.

The gate is reverse biased so that $I_G = 0$ and gate

voltage $V_G = V_2 = (V_{DD}/R_{G1} + R_{G2}) * R_{G2}$

And

$V_{GS} = v_G - v_s = V_G - I_D R_s$

The circuit is so designed that $I_D R_s$ is greater than VG so that VGS is negative. This provides correct bias voltage.

The operating point can be determined as $I_D = (V_2 - V_{GS})/ R_S$

And

$V_{DS} = V_{DD} - I_D (R_D + R_S)$

FET SMALL SIGNAL ANALYSIS

Introduction:

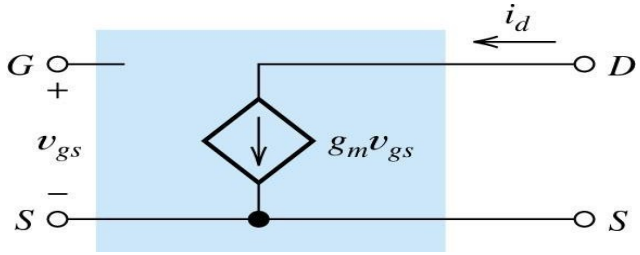
Field-effect transistor amplifiers provide an excellent voltage gain with the added feature of high input impedance. They are also considered low-power consumption configurations with good frequency range and minimal size and weight. Both JFET and

depletion MOSFET devices can be used to design amplifiers having similar voltage gains. The depletion MOSFET circuit, however, has much higher input impedance than a similar JFET configuration.

While a BJT device controls a large output (collector) current by means of a relatively small input (base) current, the FET device controls an output (drain) current by means of a small input (gate-voltage) voltage. In general, therefore, the BJT is a current-controlled device and the FET is a voltage- controlled device. In both cases, however, note that the output current is the controlled variable. Because of the high input characteristic of FETs, the ac equivalent model is somewhat simpler than that β

employed for BJTs. While the BJT had an amplification factor (beta), the FET has a transconductance factor, g_m.
The FET can be used as a linear amplifier or as a digital device in logic circuits. In fact, the enhancement MOSFET is quite popular in digital circuitry, especially in CMOS circuits that require very low power consumption. FET devices are also widely used in high-frequency applications and in buffering (interfacing) applications.

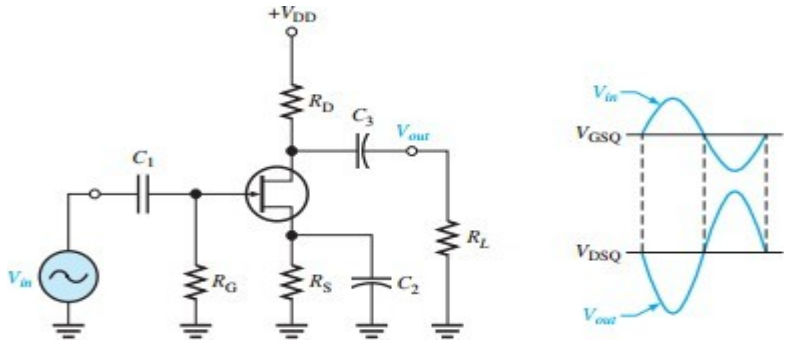
While the common-source configuration is the most popular, providing an inverted, amplified signal, one also finds common-drain (source-follower) circuits providing unity gain with no inversion and common-gate circuits providing gain with no inversion. As with BJT amplifiers, the important circuit features described in this chapter include voltage gain, input impedance, and output impedance. Due to the very high input impedance, the input current is generally Ω assumed to be 0 A and the current gain is an undefined quantity. While the voltage gain of an FET amplifier is generally less than that obtained using a BJT amplifier, the FET amplifier provides a much higher input impedance than that of a BJT configuration. Output impedance values are comparable for both BJT and FET circuits.



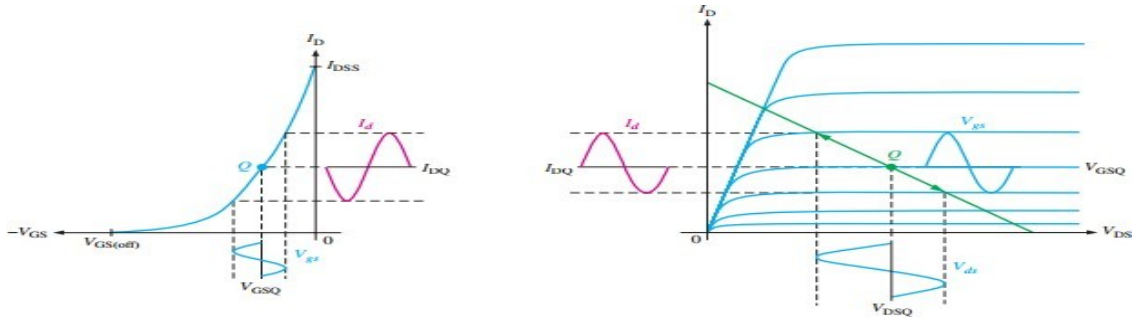
COMMON SOURCE AMPLIFIER

A common-source JFET amplifier is one in which the ac input signal is applied to the gate and the ac output signal is taken from the drain. The source terminal is common to both the input and output signal. A common-source amplifier either has no source resistor or has a bypassed source resistor, so the source is connected to ac ground. A self-biased common-source n-channel JFET amplifier with an ac source capacitively coupled to the gate is shown in Figure below. The resistor, RG, serves two purposes: It keeps the gate at approximately 0 V dc (because IGSS is extremely small), and its large value (usually several megohms) prevents

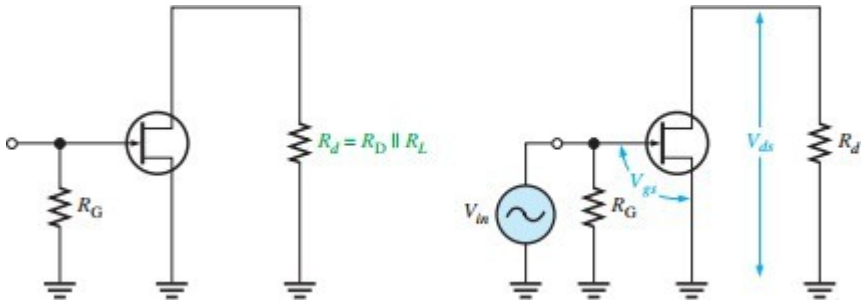
loading of the ac signal source. A bias voltage is produced by the drop across RS. The bypass capacitor, C2, keeps the source of the JFET at ac ground.



The input signal voltage causes the gate-to-source voltage to swing above and below its Q-point value (VGSQ), causing a corresponding swing in drain current. As the drain current increases, the voltage drop across RD also increases, causing the drain voltage to decrease. The drain current swings above and below its Q-point value in phase with the gate-to-source voltage. The drain-to-source voltage swings above and below its Q-point value (VDSQ) and is 180° out of phase with the gate-to-source voltage, as illustrated in Figure above. A Graphical Picture The operation just described for an n-channel JFET is illustrated graphically on both the transfer characteristic curve and the drain characteristic curve in Figure below. Part (a) shows how a sinusoidal variation, Vgs, produces a corresponding sinusoidal variation in Id. As Vgs swings from its Q-point value to a more negative value, Id decreases from its Q- point value. As Vgs swings to a less negative value, Id increases. The signal at the gate drives the drain current above and below the Q-point on the load line, as indicated by the arrows. Lines projected from the peaks of the gate voltage across to the ID axis and down to the VDS axis indicate the peak-to-peak variations of the drain current and drain-to-source voltage, as shown. Because the transfer characteristic curve is nonlinear, the output will have some distortion. This can be minimized if the signal swings over a limited portion of the load line.



AC Equivalent Circuit to analyze the signal operation of the amplifier in Figure below ,an ac equivalent circuit is as follows. Replace the capacitors by effective shorts, based on the simplifying assumption that at the signal frequency. Replace the dc source by a ground, based on the assumption that the voltage source has a zero internal resistance. The VDD terminal is at a zero-volt ac potential and therefore acts as an ac ground. The ac equivalent circuit is shown in Figure below. Notice that the VDD end of Rd and the source terminal are both effectively at ac ground. Recall that in ac analysis, the ac ground and the actual circuit ground are treated as the same point.



An ac voltage source is shown connected to the input in Figure above. Since the input resistance to a JFET is extremely high, practically all of the input voltage from the signal source appears at the gate with very little voltage dropped across the internal source resistance. Vgs = Vin. Voltage Gain The expression for JFET voltage gain that was given in Equation below applies to the common-source amplifier.

Phase Inversion The output voltage (at the drain) is out of phase with the input voltage (at the gate). The phase inversion can be designated by a negative voltage gain, Recall that the common-emitter BJT amplifier also exhibited a phase inversion.

Input Resistance is derived as follows, because the input to a common-source amplifier is at the gate, the input resistance is extremely high. Ideally, it approaches infinity and can be neglected. As you know, the high input resistance is produced by the reverse-biased PN junction in a JFET and by the insulated gate structure in a MOSFET. The actual input resistance seen by the signal source is, the gate-to-ground resistor, RG, in parallel with the FET's input resistance, VGS IGSS. The reverse leakage current, IGSS, is typically given on the datasheet for a specific value of VGS so that the input resistance of the device can be calculated.

Biasing the FET*:*

The FET can be biased as an amplifier. Consider the common source drain characteristic of a JFET. For linear amplification, Q point must be selected somewhere in the saturation region. Q point is selected on the basis of ac performance i.e. gain, frequency response, noise, power, current and voltage ratings.

Gate Bias:

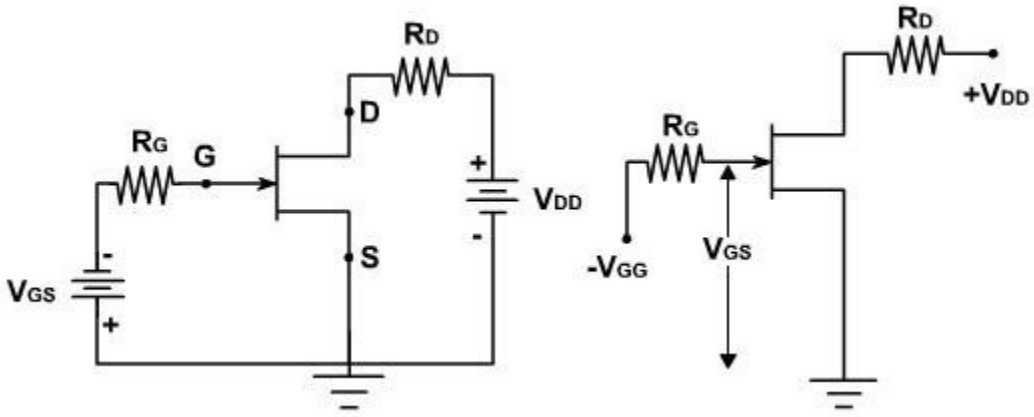


Fig.4.7, shows a simple gate bias circuit.

Separate V_{GS} supply is used to set up Q point. This is the worst way to select Q point. The reason is that there is considerable variation between the maximum and minimum values of FET parameters e.g.

	I_{DSS}	V_{GS}(off)
Minimum	4mA	-2V
Maximum	13mA	-8V

This implies that the minimum and maximum transductance curves are displaced as shown in **fig. 4.8**.

Gate bias applies a fixed voltage to the gate. This fixed voltage results in a Q point that is highly sensitive to the particular JFET used. For instance, if V_{GS}= -1V the Q point may very from Q_1 to Q_2 depending upon the JFET parameter is use.

At Q_1, I_D= 0.016 (1 - (1/8))^2 = 12.3 mA

At Q_2, I_D= 0.004 (1-(1/2))^2 = 1 mA.

The variation in drain current is very large.

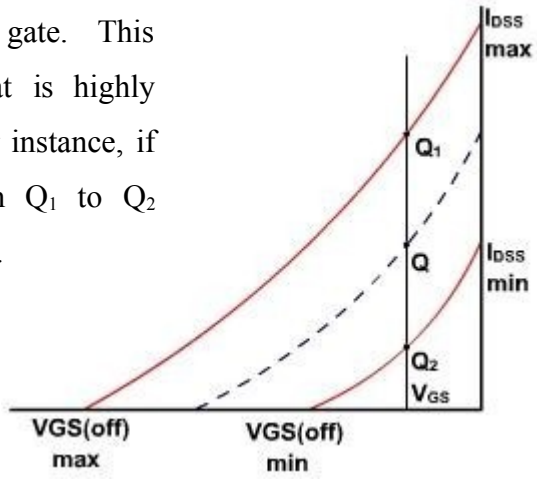
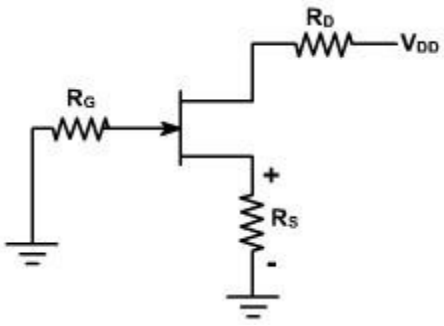


Fig. 4.8

Self Bias:

Fig. , shows a self bias circuit another way to bias a FET. Only a drain supply is used and no gate supply. The idea is to use the voltage across R_S to produce the gate source reverse voltage. This is a form of a local feedback similar to that used with bipolar transistors. If drain current increases, the voltage drop across R_S increases because the I_D R_S increases. This increases the gate source reverse voltage which makes the channel narrow and reduces the drain current. The overall effect is to partially offset the original increase in drain current. Similarly, if I_D decreases, drop across R_S decreases, hence reverse bias decreases and I_D increases.



Since the gate source junction is reverse biased, negligible gate current flows through R_G and so the gate voltage with respect to ground is zero.

$$V_G = 0;$$

The source to ground voltage equals the product of the drain current and the source resistance.

$$V_S = I_D R_S. \quad \text{(E-4.2)}$$

The gate source voltage is the difference between the gate voltage and the source voltage. $V_{GS} = V_G - V_S = 0 - I_D R_S$

$$V_{GS} = -I_D R_S. \quad \text{(E-4.3)}$$

This means that the gate source voltage equals the negative of the voltage across the source resistor. The greater the drain current, the more negative the gate source voltage becomes.

Rearranging the equation:

$$I_D = -V_{GS} / R_S \quad \text{(E-4.4)}$$

The graph of this equation is called self base line a shown in **Fig.**

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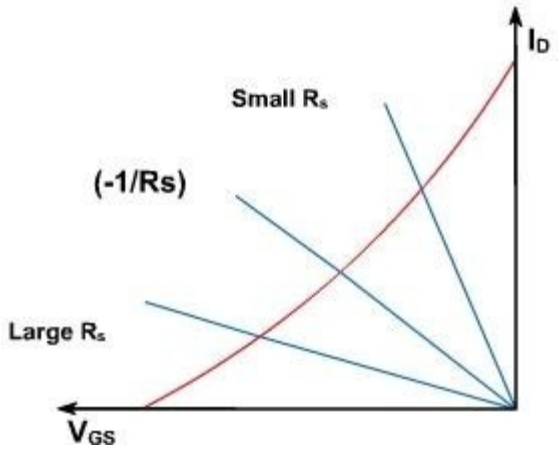
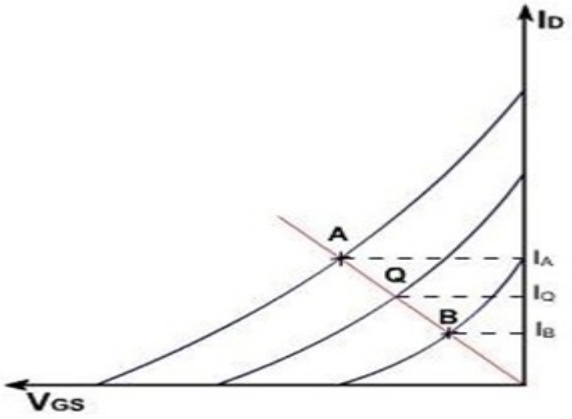


The operating point on transductance curve is the intersection of self bias line and transductance curve. The slope of the line is (-1 / R_S). If the source resistance is very large (-1 / R_S is small) then Q-point is far down the transductance curve and the drain current is small.

When R_S is small, the Q point is far up the transductance curve and the drain current is large. In between there is an optimum value of R_S that sets up a Q point near the middle of the transductance curve.

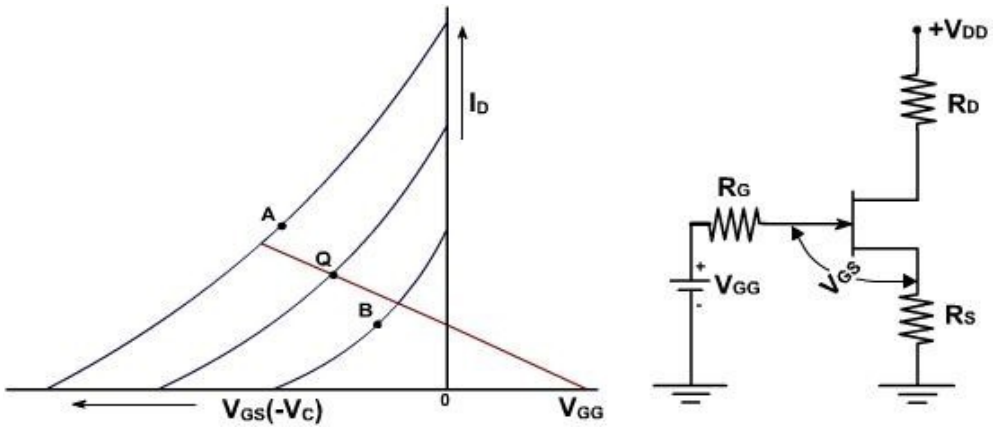
The transductance curve varies widely for FET (because of variation in I_{DSS} and $V_{GS}(off)$) as shown in **fig.** The actual curve may be in between there extremes. A and B are the optimum points for the two extreme curves. To find the optimum resistance R_S, so that Q-point is correct for all the curves, A and B points are joined such that it passes through origin.



The slope of this line gives the resistance value R_S($V_{GS} = -I_D R_S$). The current I_Q is such that $I_A > I_Q > I_B$. Here A, Q and B all points are in straight line.

Consider the case where a line drawn to pass between points A and B does not pass through the origin. The equation $V_{GS} = - I_D R_S$ is not valid. The equation of this line is $V_{GS} = V_{GG} – I_D R_S$.

Such a bias relationship may be obtained by adding a fixed bias to the gate in addition to the source self bias as shown in fig.



In this circuit.

$$V_{GG} = R_S I_G + V_{GS} + I_D R_S \qquad \text{(E-4.5)}$$

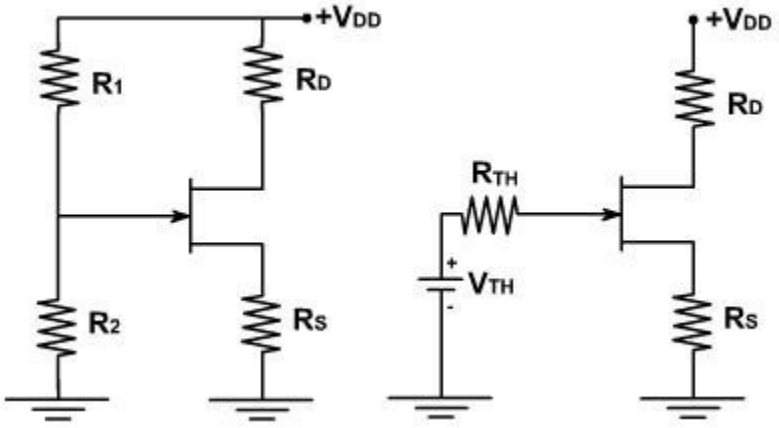
Since $R_S I_G = 0$;

$$VGG = VGS + ID\ RS$$

or $$V_{GS} = V_{GG} - I_D R_S \qquad \text{(E-4.6)}$$

Voltage Divider Bias :

The biasing circuit based on single power supply is shown in **fig.** This is similar to the voltage divider bias used with a bipolar transistor.



The Thevenin voltage V_{TH} applied to the gate is

(E-4.7)

The Thevenin resistance is given as

(E-4.8)

The gate current is assumed to be negligible. V_{TH} is the dc voltage from gate to ground.

(E-4.9)

The drain current ID is given by

(E-4.10)

and the dc voltage from the drain to ground is $V_D = V_{DD} – I_D R_D$.