Jaipur Engineering College & Research Centre, Jaipur

Lecture Notes

3EE4-06: Analog Electronics

ACADEMIC SESSION 2020-21

Prepared By:
Jisha Varghese

VISION OF ELECTRICAL ENGINEERING DEPARTMENT

Electrical Engineering Department strives to be recognized globally for outcome based knowledge and to develop human potential to practice advance technology which contribute to society.

MISSION OF ELECTRICAL ENGINEERING DEPARTMENT

M1. To impart quality technical knowledge to the learners to make them globally competitive Electrical Engineers.

M2. To provide the learners ethical guidelines along with excellent academic environment for a long productive career.

M3. To promote industry-institute relationship.

PROGRAM OUTCOMES

1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems in Electrical Engineering.
2. **Problem analysis:** Identify, formulate, research literature, and analyze complex engineering problems reaching substantial conclusions using first principles of mathematics, natural sciences, and engineering sciences in Electrical Engineering.
3. **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations using Electrical Engineering.
4. **Conduct investigations of complex problems:** Use research based knowledge and research methods including design of experiments, analysis and interpretation of data and synthesis of the information to provide valid conclusions using Electrical Engineering.
5. **Modern tool usage:** Create, select and apply appropriate techniques, resources, and modern engineering and EE tools including prediction and modeling to complex engineering activities with an understanding of the limitations in EE.
6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice using EE.
7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of EE and need for sustainable development in EE.
8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice using EE.
9. **Individual and team work:** Function effectively as an individual and as a member or leader in diverse teams, and multi-disciplinary settings in EE.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations and give and receive clear instructions.
11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage EE projects and in multi-disciplinary environments.
12. **Life-long learning:** Recognize the need for and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological changes needed in EE.

COURSE OUTCOMES:

On successful completion of the course, the students will be able to: -

CO1	Understand the characteristics of Diodes, concepts behind the Clippers, and Clampers. Design and analysis of various rectifier and amplifier circuits
CO2	Analyze the characteristics of current flow in a bipolar junction transistor and MOSFET & different electronic devices such as Amplifiers
CO3	Understand the dynamics of Linear & Non Linear Devices

Syllabus

RAJASTHAN TECHNICAL UNIVERSITY, KOTA

SYLLABUS

2nd Year - III Semester: B.Tech. (Electrical Engineering)

3EE4-06: Analog Electronics

Credit: 3 | **Max. Marks: 150 (IA:30, ETE:120)**
3L+0T+0P | **End Term Exam: 3 Hours**

SN		Hours
1.	**Diode circuits** P-N junction diode, I-V characteristics of a diode; review of half-wave and full-wave rectifiers, Zener diodes, clamping and clipping circuits.	4
2.	**BJT circuits** Structure and I-V characteristics of a BJT; BJT as a switch. BJT as an amplifier: small-signal model, biasing circuits, current mirror; common-emitter, common-base and common collector amplifiers; Small signal equivalent circuits, high-frequency equivalent circuits.	8
3.	**MOSFET circuits** MOSFET structure and I-V characteristics. MOSFET as a switch. MOSFET as an amplifier: small-signal model and biasing circuits, common-source, common-gate and common-drain amplifiers; small signal equivalent circuits - gain, input and output impedances, transconductance, high frequency equivalent circuit.	8
4.	**Differential, multi-stage and operational amplifiers** Differential amplifier; power amplifier; direct coupled multi-stage amplifier; internal structure of an operational amplifier, ideal op-amp, non-idealities in an op-amp (Output offset voltage, input bias current, input offset current, slew rate, gain bandwidth product)	8
5.	**Linear applications of op-amp** Idealized analysis of op-amp circuits. Inverting and non-inverting amplifier, differential amplifier, instrumentation amplifier, integrator, active filter, P, PI and PID controllers and lead/lag compensator using an op-amp, voltage regulator, oscillators (Wein bridge and phase shift). Analog to Digital Conversion.	8
6.	**Nonlinear applications of op-amp** Hysteretic Comparator, Zero Crossing Detector, Square-wave and triangular-wave generators, Precision rectifier, peak detector. Monoshot	6
	TOTAL	**42**

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Unit: 2

Chapter: BJT Circuits

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Unit-2 (BJT circuits)

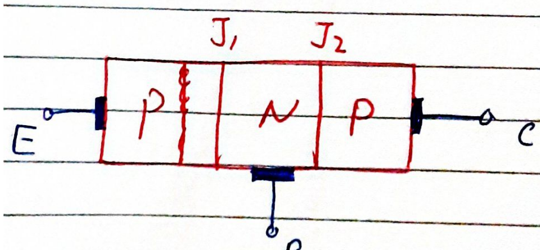
BJT :- (Bipolar Junction Transistor) is a two junctions, bi-polar, 3-termial device which is basically used as an amplifier when working in active mode and working as a switch when working in cut off or Saturation mode.

Construction :-

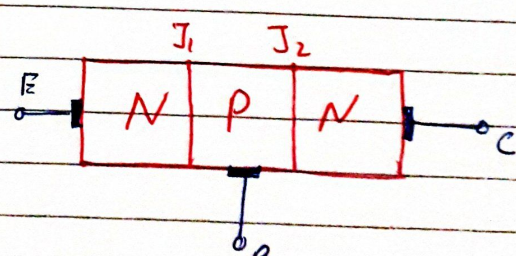
It has 2 junction (J_1 and J_2), three terminal device. The current is carried either by holes or electrons (Bipolar → both e^- & holes participates in injection process)

The 3 terminals formed are Emitter (E), Base (B) and collector (C).
It is of two types

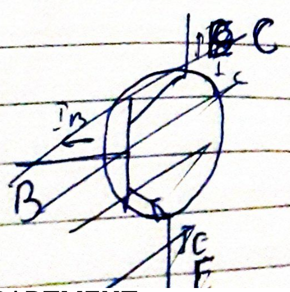
① NPN ② PNP

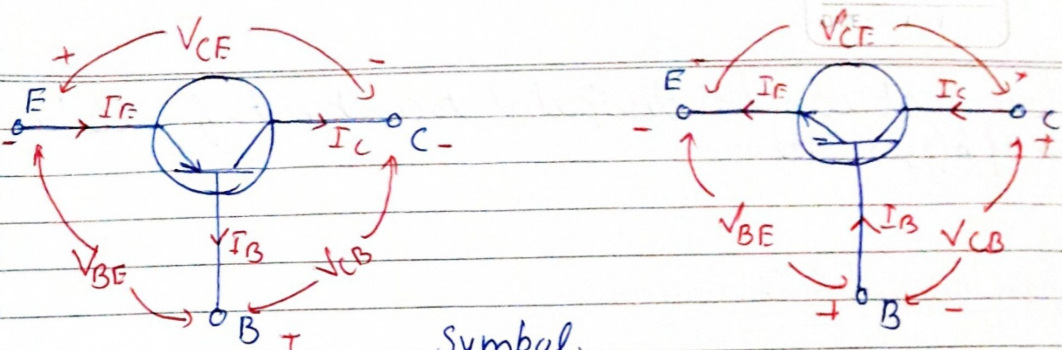


PNP Transistor



NPN Transistor





Symbol.

Transitor has 3 layers

1) Emitter :- Most heavily doped. It emits charges.

2) Base :- Central portion of transistor. Doping level & Size is Kept minimum due to following reason.

1) Concentration of charge carriers in base ~~will be~~ is less (due to low doping), hence the recombination rate decreases and the amount of charge carriers entering into collector increases.

~~3)~~ 2) With thin base, the charges injected from emitter will come in contact with lesser number of opposite charge carriers of base and recombination rate will decrease.

$$\text{Resistivity} \propto \frac{1}{\text{Doping level}}$$

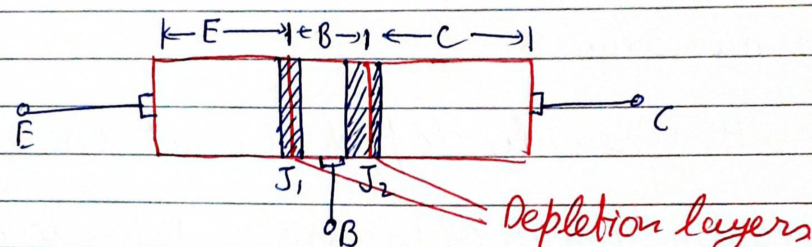
Small crosssection area of base, maximum resistance.

3) Collector :- Size of collector is larged due to

1) No. of charge carriers collected increases with size of collector
2) Transistor amplification factor $\alpha, \beta \uparrow$ with $\uparrow$ in number of collected charges
3) Heat generated across collector Junction is more,

More heat can be dissipated to ambient if collector is if bigger size.

Open Circuited Transistor :-



Width of depletion layer is inversely proportional to doping concentration. Hence peneration of depletion layer is more in base.

Operating region :-

a) Active Region :- E-B → F.B , B-C → R.B , $I_C = \beta . I_b$

b) Cut-off Region :- Both junction are reverse biased (Fully OFF) $I_C = I_{(Sat)}$

c) Saturation Region :- Both junctions are F.B (Fully ON) $I_C = 0$

Transistor Operation :-

Let us consider a ~~DEKHP~~ N-P-N transistor such that E-B junction is F.B & C-B junction is R.B.

Since the E-B junction is forward biased, the depletion layer between E-B Junction disappears

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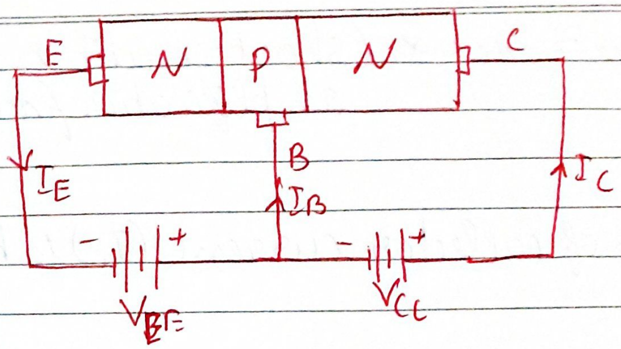

e^- from emitter junctions repelles the -ve terminal of battery and diffuse into base. To a small amount recombination occurs at Base junction due to which a small amount of Base current flows through the ckt (μA).

C-B junction is reverse biased, hence the remaining e^- in base region are attracted towards collector and hence collector current I_c flows.

$\therefore \boxed{I_E = I_B + I_C}$

Current Gains -

1) Alpha (α)

Ratio of collector current I_c to emitter current I_E.

$$\boxed{\alpha_{dc} = \frac{I_C}{I_E}}$$

α varies from 0.90 to 0.998.

$$\boxed{\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB} = \text{constant}}}$$

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$\therefore \alpha_{ac} \cong \alpha_{dc} = \alpha$ (Short circuit current amplification factor)

2) Beta(β)

Ratio of collector current (I_C) to base current (I_B).

$$\boxed{\beta_{dc} = \frac{I_C}{I_B}}$$

β ranges from 50 to more than 400.

$$\boxed{\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE} = \text{constant}}}$$

$\beta_{dc} = \beta_{ac} = \beta$ (current amplification factor)

Relation between α & β

$$\beta = \frac{\Delta I_C}{\Delta I_B} \qquad \alpha = \frac{\Delta I_C}{\Delta I_E}$$

Now

$$I_E = I_B + I_C$$

Let Δ be the small change

$$\therefore \Delta I_E = \Delta I_B + \Delta I_C$$

$$\Delta I_B = \Delta I_E - \Delta I_C$$

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

Sub. the Value of ΔI_B in above equation

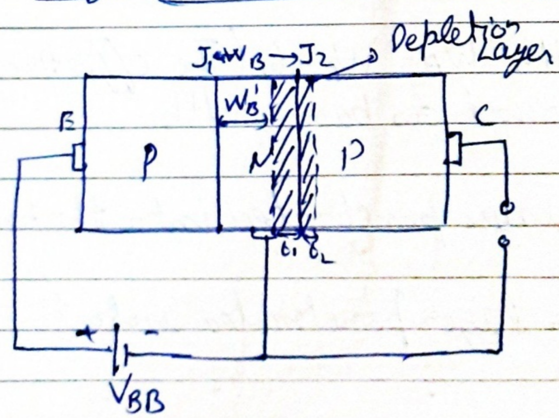
$$\beta = \frac{\Delta I_C}{\Delta I_E - \Delta I_C} = \frac{\Delta I_C / \Delta I_E}{1 - \frac{\Delta I_C}{\Delta I_E}}$$

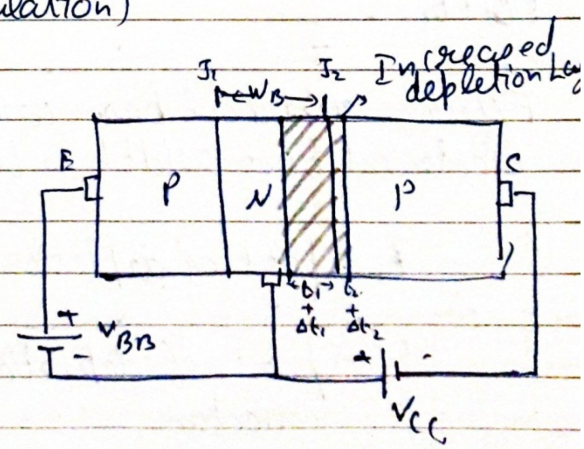
$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

||y

$$\boxed{\alpha = \frac{\beta}{1+\beta}}$$

Early Effect (Base Width Modulation)





Increasing reverse bias across collector base junction reduces effective electrical width of base. This is called Early Effect.

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From the above figure, let W be the width of depletion layer which is dependant on the concentration of doping N and applied reverse voltage V_R.

Thickness of depletion layer

$$W \propto \left(\frac{V_\gamma + V_R}{N}\right)^{1/2} \qquad V_\gamma = \text{Cutin voltage}$$

~~Thic~~ ~~Ad con~~

Thickness of depletion layer $\propto \frac{1}{\sqrt{N}}$

Where N = concentration of doping
$N = N_A$ for P-type $= N_D$ for N type.

For unbiased junction J_2. Width of depletion layer is $(t_1 + t_2)$

Effective electrical base width $W_B' = W_B - t_1$ (The effective electrical base width is termed as base width.

$t_1 \rightarrow$ part of depletion layer penetrated into the base.

$t_2 \rightarrow$ part of depletion layer penetrated into the collector.

$t_1 \gg t_2$. (Since base is lightly doped in comparison with collector)

With increase in reverse bias 't_1' and 't_2' increases to $t_1 + \Delta t_1$ & $t_2 + \Delta t_2$ resp.

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Now $\Delta t_1 >> \Delta t_2$ (dopping of level of collector is much higher than base)

effective electrical base width $W''_B = W_B - (t_1 + \Delta t_1)$

With ↑ in R.B, thickness of depletion width increases and it penetrates into base and collector region, but penetration into base region, is much larger than the collector region and effective electrical base width is reduced to W''_B

$$W''_B = W_B - (t_1 + \Delta t_1)$$

Change of reverse bias at collector junction modulates (change) the effective electrical width of the base, this is known as Base width modulation or Early effect.

Coupling Capacitor (C_c)

→ Used to couple o/p of one stage to i/p of next stage. It offers very high impedance to D.C and very low impedance to A.C. s/g.

→ If not done the bias condition of next stage will be drastically changed due to shunting effect of R_c. R_c comes in parallel with i/p imp of next stage, altering the biasing condition.

→ C_c isolates D.C. of one stage from next stage, but allows the passage of AC s/g.

Emitter Bypass Capacitor (C_c)

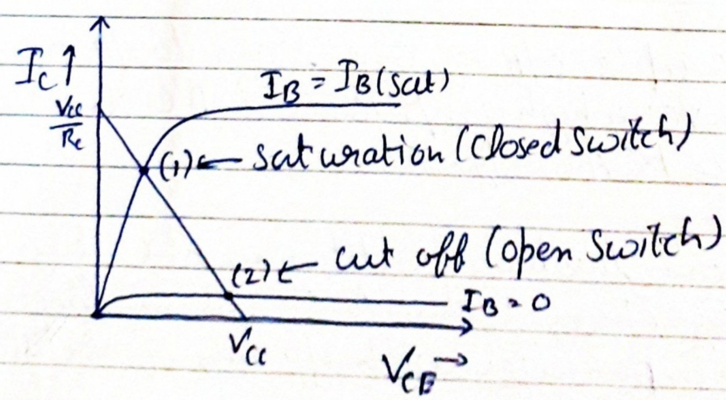
→ It is used to bypass emitter resistance R_E for A.C. S/s. Voltage drop ($I_E R_E$) across R_E is a -ve feedback to i/p ckt, hence gain reduce.

→ In order to avoid the decrease in the gain I_E should not be bypassed through R_E. The C_E connected in parallel with R_E behaves as short ckt, I_E is bypassed through S.C. path and voltage drop ($I_E R_E$) is reduced to zero.

→ Hence overall A.C. Gain increases.

C_E → Large enough so that act as SC → Low freq.
OC → for DC S/s.

BJT as Switch :-



O/P characteristics of transistor

Let m be the slope.

$$\text{Slope}(m) = \frac{dI_c}{dV_c} \text{ (very high)}$$

o/p resistance of transistor, $R_O = \frac{dV_C}{dI_C} = \frac{1}{m} \to 0$

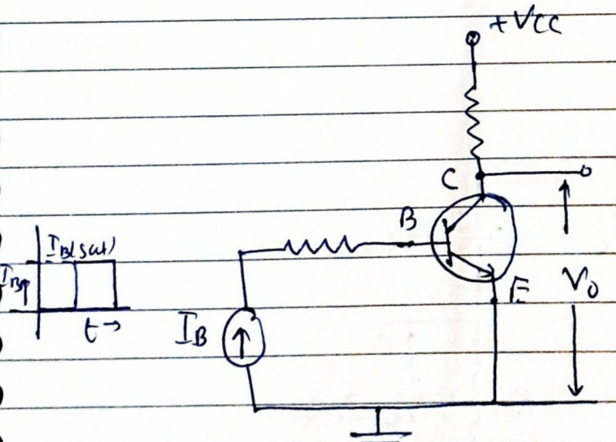
therefore transistor offers zero resistance in saturation region and act like a closed switch.

When Base current (I_B) is zero, the point of operation of transistor will be point (2).

$m \simeq 0.$

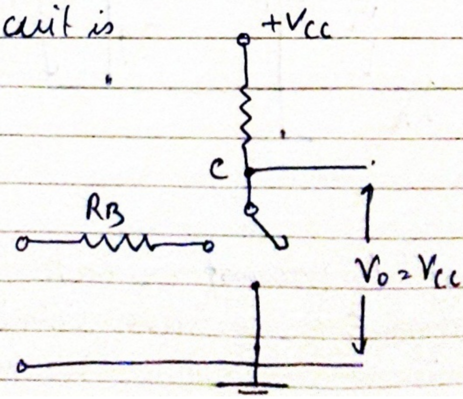
$$R_O = \frac{dV_C}{dI_C} = \frac{1}{m} \to \infty$$

Transistor offers very high impedance and acts like an open switch in cut off region.



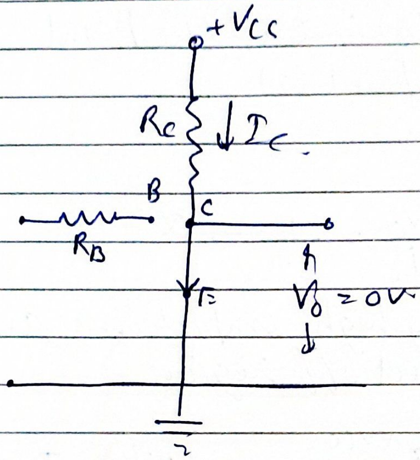
When I_B is zero, transistor is cutoff, collector current (I_C) is zero. & $V_O = V_{CC}$.

Hence the circuit is

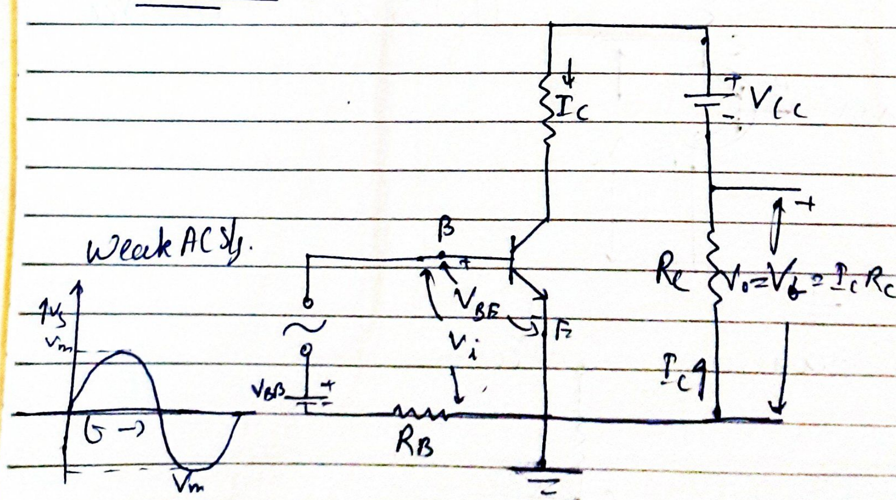


When I_B is equal to $I_{B(sat)}$, the transistor is driven into saturation and I_C is max. and equal to V_{CC}/R_C.

$$V_0 = V_{CC} - I_C R_C \approx 0 \quad \text{(S.C. or closed switch)}$$



BJT as Amplifier



A transistor is used to transfer weak s/g from low i/p resistive ckt to high o/p resistive circuit.

Transistor is operated in active region with the help of biasing batteries V_{BB} & V_{CC}. The i/p s/g is applied across Base(B) and emitter(E) while o/p is taken across R_C.

As we know, that the i/p resistance is low, due to which there is a change in I_B when a small change in i/p s/g occurs..

This change in I_B cause a large change in I_C, by relatio

$$\boxed{I_C = \beta I_B}$$

Due to which their is a large drop across R_C & Hence a weak s/g is being amplified.

Derivation

Let V_s be the AC s/g. Let V_i be the i/p s/g applied between Base(B) and Emitter(E)

$$\therefore \; V_i = V_S + V_{BB}$$

$V_{BB} \rightarrow$ DC biasing battery.

Let ΔV_i be the change in the i/p s/g.

$$\Delta V_i = V_s.$$

Let $I_C \rightarrow$ D.C component
$i_c \rightarrow$ A.C. Component.

Hence variation in collector current will be only due to A.C. component (i_c)

$$\Delta I_C = i_c$$

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$$\Delta V_L = -\Delta I_C R_C - i_C R_C$$

Voltage gain $= \dfrac{\Delta \text{ o/p volt}}{\Delta \text{ i/p volt}}$

$$A_V = \frac{\Delta V_L}{\Delta V_i} = \frac{-i_C R_C}{V_S} = -\frac{\beta i_b R_C}{V_S}$$

$$= -\frac{\beta R_C}{V_S/i_b} = \frac{-\beta R_C}{r_b}$$

$r_b = \dfrac{V_S}{i_b}$ = i/p base circuit resistance.

$\beta >> 1$, $R_C >> r_b$

$A_V >> 1$

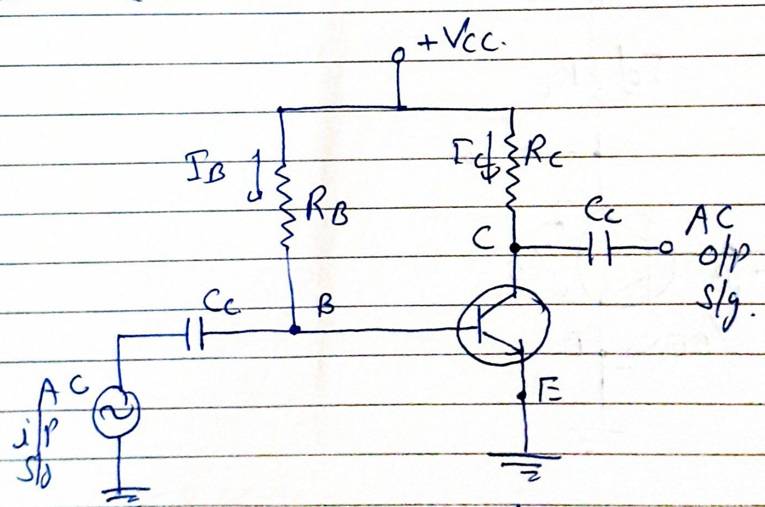
Hence transistor act like an amp.

Biasing of BJT

* Transistor operates mainly in linear region of o/p characteristics, where o/p voltage is linear function of i/p voltage.

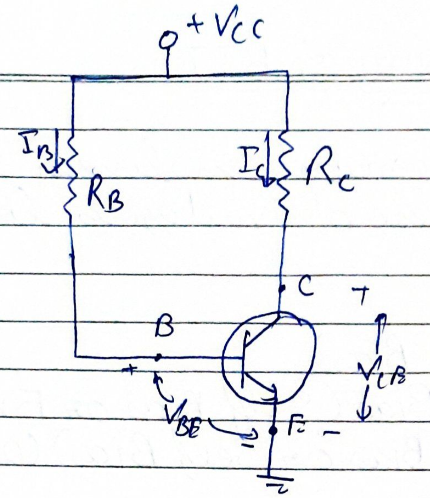
① Base Bias (Fixed Bias)
② Voltage divider Bias (Self Bias or Emitter Bias)
③ (Voltage Feedback Bias or Self Bias) (Collector Feedback

Fixed Bias (Base Bias)

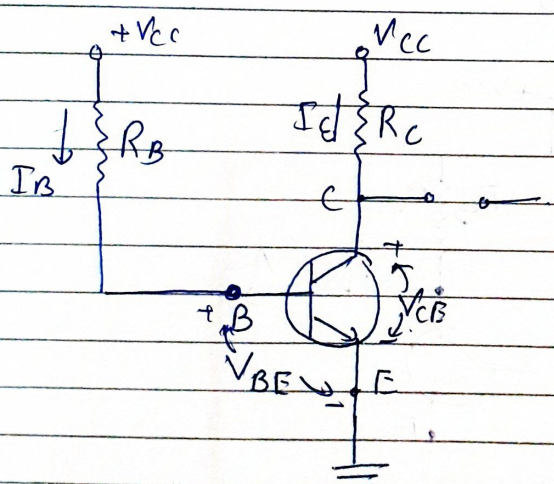


Assumptions:-

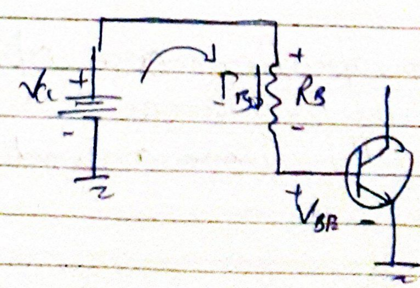
① Coupling capacitors are open circuited.
② remove all AC sources
Applying the above assumption in the circuit.



Seperating i/p & o/p ckts.



① Base emitter ckt.



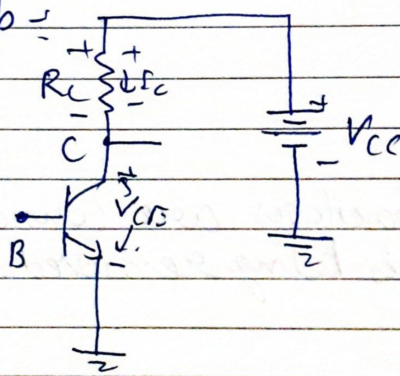
Applying KVL in clockwise direction.

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

$$V_{CC} - V_{BE} = I_B R_B$$

$$\therefore \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}} \quad —①$$

② collector Emitter Loop :-



As we know $\boxed{I_C = \beta I_B}$ —②

Applying KVL across O/P

$$+V_{CC} - I_C R_C - V_{CE} = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C} \quad —③$$

V_{CE} can also be written as

$$\boxed{V_{CE} = V_C - V_E}.$$

Since Emitter (E) is ground $V_E = 0$

$$\therefore \boxed{V_{CE} = V_C}$$

||ly $V_{BE} = V_B - V_E$

$$\boxed{V_{BE} = V_B}$$

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Voltage Divider Bias

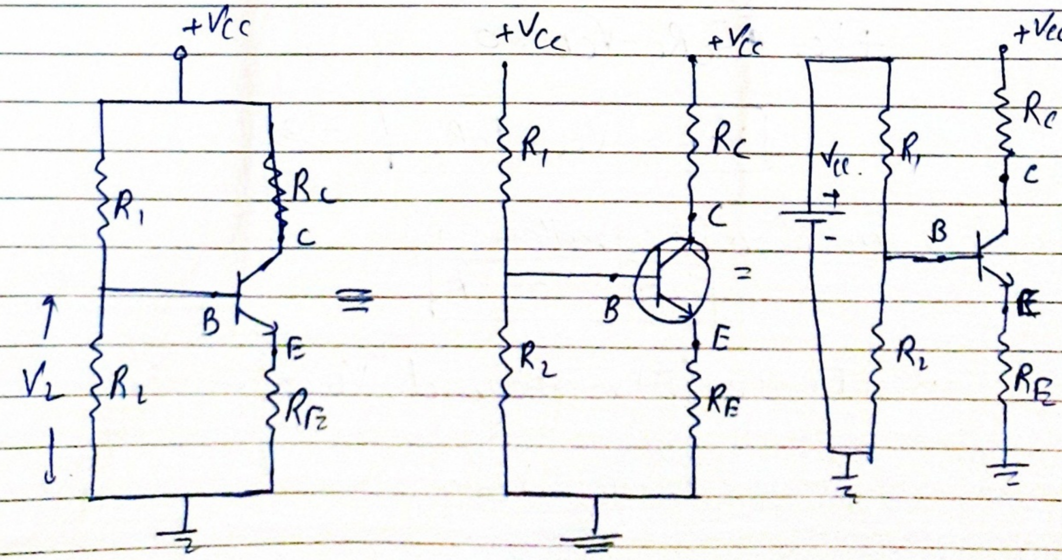
* Independent of B of transistor.

* Resistor R_1 and R_2 forms the voltage divider circuit. Biasing voltage V_{cc} is divided into two parts and voltage drop V_2 across R_2 is applied between base and emitter to forward bias the emitter base junction

* Biasing voltage is obtained through voltage divider circuit

Analysis:-

Capacitors are considered as open circuit and AC s/g is being removed. The circuit simplified as



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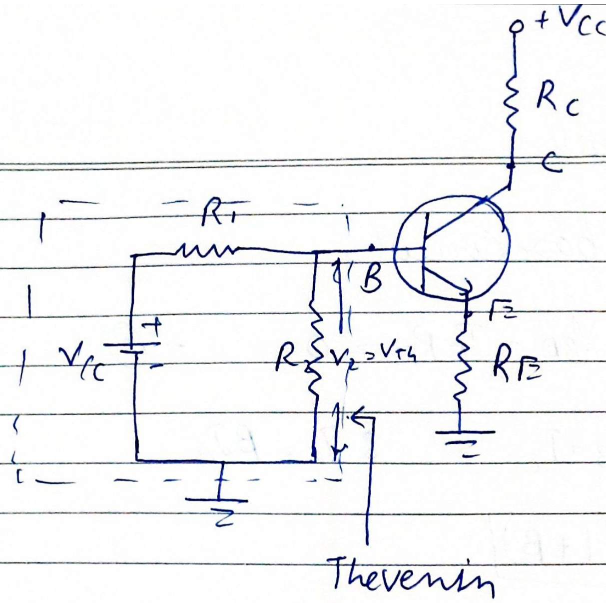
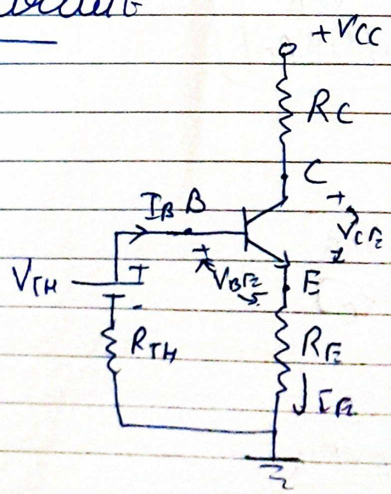


R_{TH} = (Thevenin Resistance) = $\boxed{R_1 \| R_2 = R_{TH}}$

$E_{TH} = V_{R2} = I R_2 = \boxed{\dfrac{V_{CC} \cdot R_2}{R_1 + R_2} = V_{TH}}$ $\left\{ I = \dfrac{V_{CC}}{R_1 + R_2} \right\}$

Thevenized circuit



Mathematical Analysis :-

Applying KVL to the base circuit.

$$-I_B R_{th} + V_{th} - V_{BE} - I_E R_E = 0 \qquad -(1)$$

Since $I_E = I_B + I_C$ & $I_C = \beta I_B$

$$\boxed{I_E = I_B(1+\beta)}$$

sub. this value in eq. (1)

$$-I_B R_{th} + V_{th} - V_{BE} - I_B(1+\beta)R_E = 0$$

$$V_{TH} = V_{BE} + I_B[R_{th} + (1+\beta)R_E]$$

$$\boxed{I_B = \frac{V_{TH} - V_{BE}}{[R_{TH} + (1+\beta)R_E]}}$$

$$I_C = \beta I_B$$

$$= \frac{\beta[V_{TH} - V_{BE}]}{[R_{TH} + (1+\beta)R_E]}$$

$$= \frac{V_{th} - V_{BE}}{R_E + \frac{R_E + R_{th}}{\beta}}$$

$$\beta >> 1 \Rightarrow R_E >> \frac{R_E + R_{th}}{\beta}$$

$$I_{CQ} = I_C = \frac{V_{TH} - V_{BE}}{R_E}$$

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$\because V_{th} >> V_{BE}$

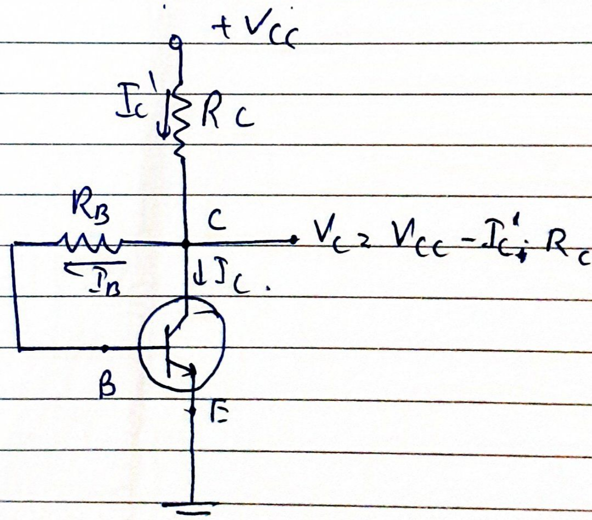
$$I_{CQ} = \frac{V_{TH}}{R_E}$$

$$V_{CEQ} = V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$= V_{CC} - I_C(R_C + R_E)$$

$$\boxed{V_{CE} = V_{CC} - I_{CQ}(R_C + R_E)}$$

Collector Feedback Bias (Voltage Feedback Bias or Self Bias)



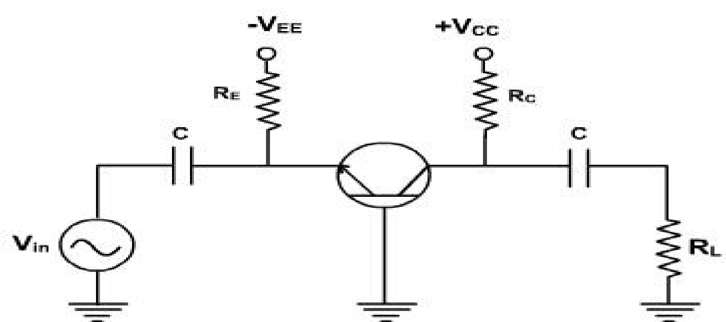
* R_B helps in compensating the variation in I_c due to change in temperature.

$\beta \uparrow$ with rise in temperature.

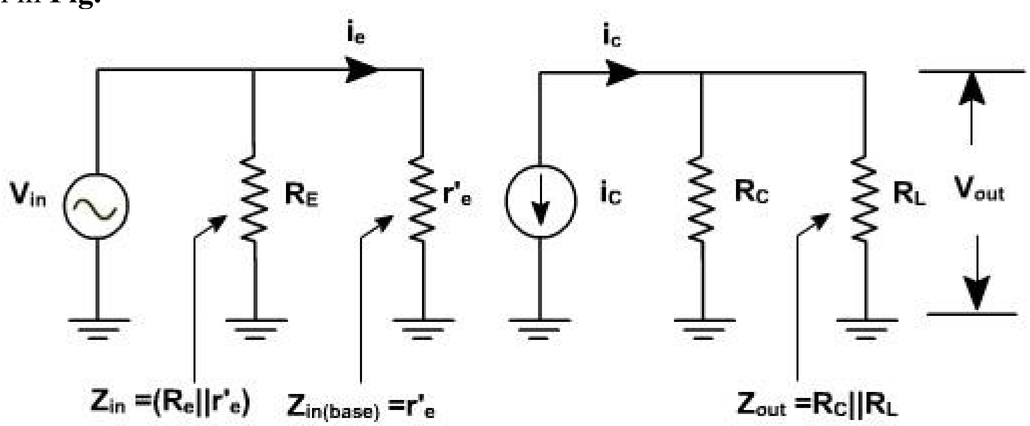
Common Base Amplifier:

The common base amplifier circuit is shown in **Fig.** The V_{EE} source forward biases the emitter diode and V_{CC} source reverse biased collector diode. The ac source v_{in} is connected to emitter through a coupling capacitor so that it blocks dc. This ac voltage produces small fluctuation in currents and voltages. The load resistance R_L is also connected to collector through coupling capacitor so the fluctuation in collector base voltage will be observed across R_L. The dc equivalent circuit is obtained by reducing all ac sources to zero and opening all capacitors. The dc collector current is same as I_E and V_{CB} is given by

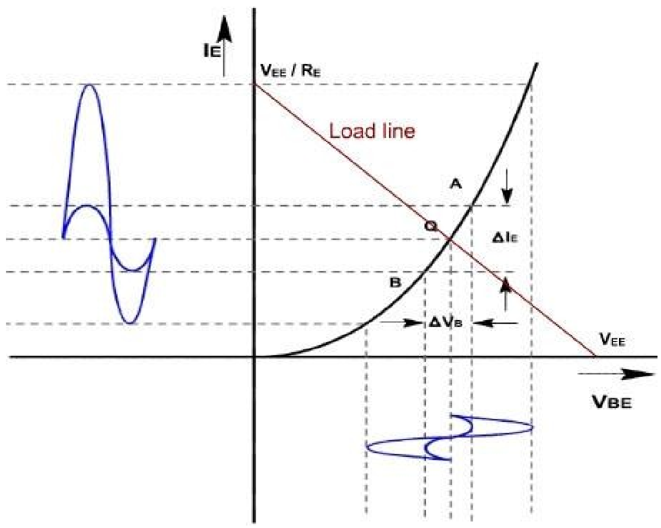
$$V_{CB} = V_{CC} - I_C R_C.$$



These current and voltage fix the Q point. The ac equivalent circuit is obtained by reducing all dc sources to zero and shorting all coupling capacitors. r'e represents the ac resistance of the diode as shown in **Fig.**



the diode curve relating I_E and V_{BE}. In the absence of ac signal, the transistor operates at Q point (point of intersection of load line and input characteristic). When the ac signal is applied, the emitter current and voltage also change. If the signal is small, the operating point swings sinusoidally about Q point (A to B).



If the ac signal is small, the points A and B are close to Q, and arc A B can be approximated by a straight line and diode appears to be a resistance given by

$$r'_e = \left.\frac{\Delta V_{BE}}{\Delta I_E}\right|_{\text{small change}}$$

$$= \frac{V_{be}}{i_e} = \frac{\text{ac voltage across base and emitter}}{\text{ac current through emitter}}$$

If the input signal is small, input voltage and current will be sinusoidal but if the input voltage is large then current will no longer be sinusoidal because of the non linearity of diode curve. The emitter current is elongated on the positive half cycle and compressed on negative half cycle. Therefore the output will also be distorted.

r'_e is the ratio of ΔV_{BE} and ΔI_E and its value depends upon the location of Q. Higher up the Q point small will be the value of r' e because the same change in V_{BE} produces large change in I_E.

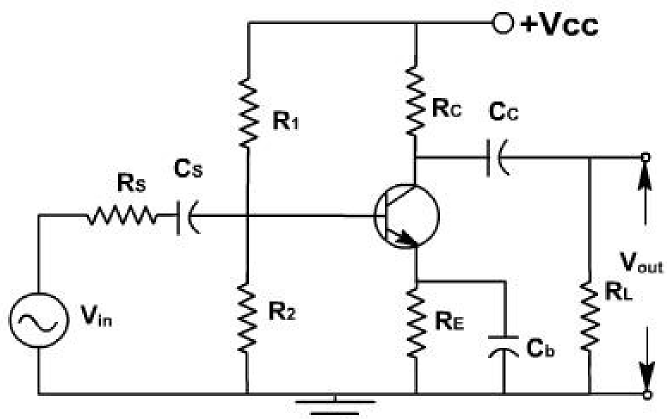
$$r'_e = 25mV / I_E$$

Small Signal CE Amplifiers

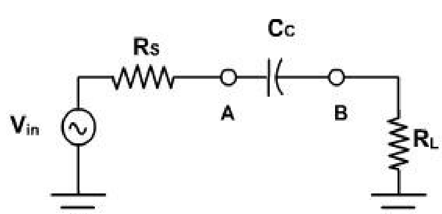
CE amplifiers are very popular to amplify the small signal ac. After a transistor has been biased with a Q point near the middle of a dc load line, ac source can be coupled to the base. This produces fluctuations in the base current and hence in the collector current of the same shape and frequency. The output will be enlarged sine wave of same frequency.

The amplifier is called linear if it does not change the wave shape of the signal. As long as the input signal is small, the transistor will use only a small part of the load line and the operation will be linear.

On the other hand, if the input signal is too large. The fluctuations along the load line will drive the transistor into either saturation or cut off. This clips the peaks of the input and the amplifier is no longer linear.



The coupling capacitor (C_C) passes an ac signal from one point to another. At the same time it does not allow the dc to pass through it. Hence it is also called blocking capacitor.



The ac voltage at point A is transmitted to point B. For this series reactance X_C should be very small compared to series resistance R_S. The circuit to the left of A may be a source and a series resistor or may be the Thevenin equivalent of a complex circuit. Similarly R_L may be the load resistance or equivalent resistance of a complex network. The current in the loop is given by

$$i = \frac{v_{in}}{\sqrt{(R_S + R_L)^2 + X_C^2}}$$

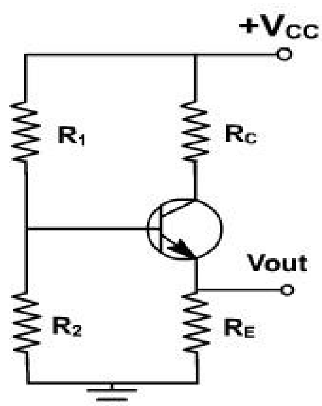
$$= \frac{v_{in}}{\sqrt{R^2 + X^2}}$$

Analysis of CE amplifier:

In a transistor amplifier, the dc source sets up quiescent current and voltages. The ac source then produces fluctuations in these current and voltages. The simplest way to analyze this circuit is to split the analysis in two parts: dc analysis and ac analysis. One can use superposition theorem for analysis .

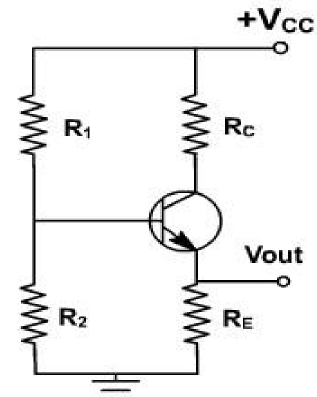
AC & DC Equivalent Circuits:

For dc equivalent circuit, reduce all ac voltage sources to zero and open all ac current sources and open all capacitors.



AC Load line:

Consider the dc equivalent circuit



Assuming $I_C = I_C$(approx), the output circuit voltage equation can be written as

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$\text{and} \quad I_C = -\frac{V_{CE}}{R_C + R_E} + \frac{V_{CC}}{R_C + R_E}$$

$$V_{CE} = 0, \quad I_C = \frac{V_{CC}}{R_C + R_E}$$

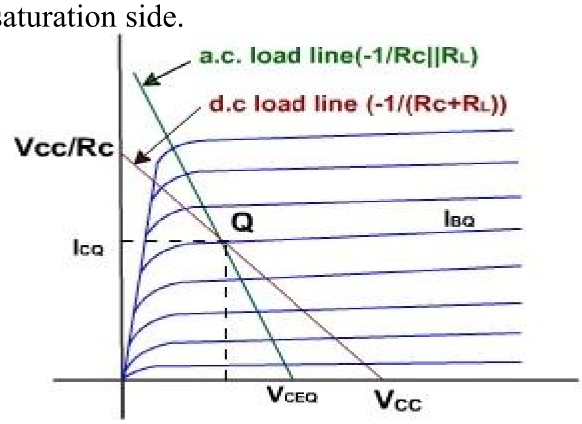
$$\text{and} \quad I_C = 0, \quad V_{CE} = V_{CC} \qquad \text{(E-51)}$$

The slop of the d.c load line is

$$-\frac{1}{R_C + R_E}$$

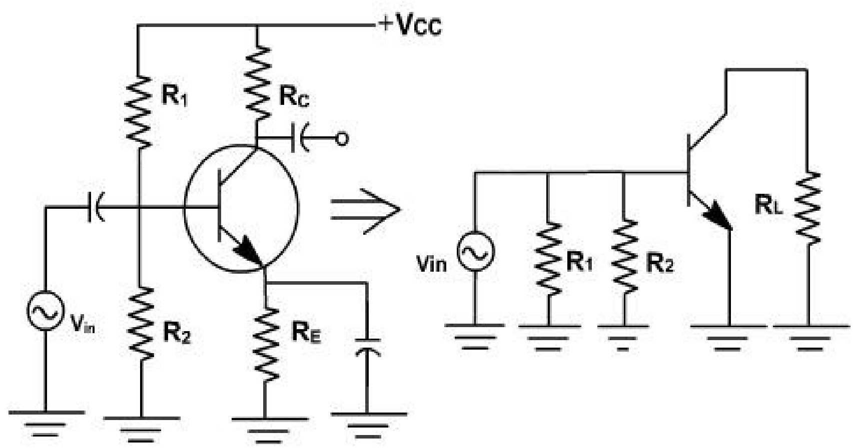
.

When considering the ac equivalent circuit, the output impedance becomes $R_C \parallel R_L$ which is less than (R_C+R_E). In the absence of ac signal, this load line passes through Q point. Therefore ac load line is a line of slope (-1 / ($R_C \parallel R_L$)) passing through Q point. Therefore, the output voltage fluctuations will now be corresponding to ac load line as shown in **fig.** Under this condition, Q-point is not in the middle of load line, therefore Q- point is selected slightly upward, means slightly shifted to saturation side.



Voltage gain:

To find the voltage gain, consider an unloaded CE amplifier. The ac equivalent circuit is shown in **fig**. The transistor can be replaced by its collector equivalent model i.e. a current source and emitter diode which offers ac resistance r'_e.



The input voltage appears directly across the emitter diode

Therefore emitter current $i_e = V_{in} / r'_e$.

Since, collector current approximately equals emitter current and $i_C = i_e$ and $v_{out} = - i_e R_C$ (The minus sign is used here to indicate phase inversion)

Further $v_{out} = - (V_{in} R_C) / r'_e$

Therefore voltage gain $A = v_{out} / v_{in} = -R_C / r'_e$

The ac source driving an amplifier has to supply alternating current to the amplifier. The input impedance of an amplifier determines how much current the amplifier takes from the ac source.

In a normal frequency range of an amplifier, where all capacitors look like ac shorts and other reactance are negligible, the ac input impedance is defined as

$$z_{in} = v_{in} / i_{in}$$

Where v_{in}, i_{in} are peak to peak values or rms values

The impedance looking directly into the base is symbolized $z_{in\ (base)}$ and is given by

$$Z_{in(base)} = v_{in} / i_b ,$$

Since, $v_{in} = i_e r'_e$

From the ac equivalent circuit, the input impedance z_{in} is the parallel combination of R_1 , R_2 and β

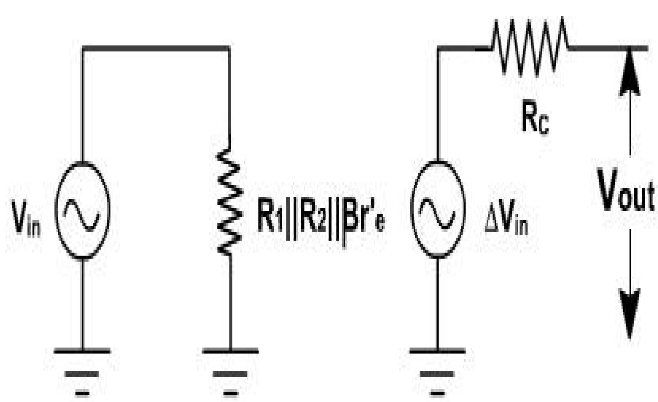
$$r'_e.\ Z_{in} = R_1 \parallel R_2 \parallel \beta r'_e$$

The Thevenin voltage appearing at the output is

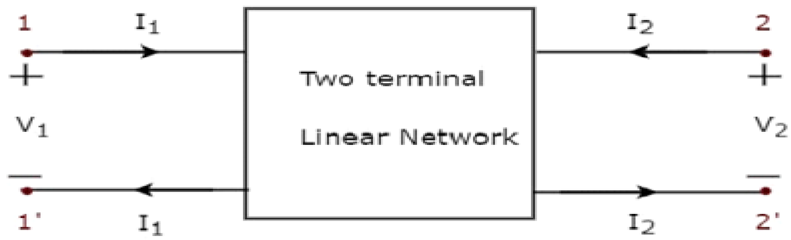
$$v_{out} = A\ v_{in}$$

The Thevenin impedance is the parallel combination of R_C and the internal impedance of the current source. The collector current source is an ideal source, therefore it has an infinite internal impedance.

$$z_{out} = R_C.$$



Two port network is a pair of two terminal electrical network in which, current enters through one terminal and leaves through another terminal of each port. Two port network representation is shown in the following figure.



Here, one pair of terminals, 1 & 1' represents one port, which is called as **port1** and the other pair of terminals, 2 & 2' represents another port, which is called as **port2**.

There are **four variables** V_1, V_2, I_1 and I_2 in a two port network as shown in the figure. Out of which, we can choose two variables as independent and another two variables as dependent. So, we will get six possible pairs of equations. These equations represent the dependent variables in terms of independent variables. The coefficients of independent variables are called as **parameters**. So, each pair of equations will give a set of four parameters.

h-parameters

We will get the following set of two equations by considering the variables V_1 & I_2 as dependent and I_1 & V_2 as independent. The coefficients of independent variables, I_1 and V_2, are called as **h-parameters**.

$$V_1 = h_{11}I_1 + h_{12}V_2$$

$$I_2 = h_{21}I_1 + h_{22}V_2$$

The h-parameters are

$$h_{11} = \frac{V_1}{I_1}, \; when \; V_2 = 0$$

$$h_{12} = \frac{V_1}{V_2}, \; when \; I_1 = 0$$

$$h_{21} = \frac{I_2}{I_1}, \; when \; V_2 = 0$$

$$h_{22} = \frac{I_2}{V_2}, \; when \; I_1 = 0$$

h-parameters are called as **hybrid parameters**. The parameters, h_{12} and h_{21}, do not have any units, since those are dimension-less. The units of parameters, h_{11} and h_{22}, are Ohm and Mho respectively.

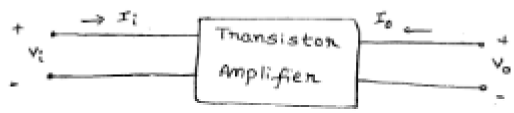
We can calculate two parameters, h_{11} and h_{21} by doing short circuit of port2. Similarly, we can calculate the other two parameters, h_{12} and h_{22} by doing open circuit of port1.

The h-parameters or hybrid parameters are useful in transistor modelling circuits (networks).

BJT AMPLIFIERS

H-Parameter Representation of a Transistor

A transistor can be treated as a two-port Network



Here I_i = Input current to the Amplifier

V_i = Input voltage to the Amplifier

I_o = Output current of the Amplifier

V_o = output voltage of the Amplifier

Transistor is a current operated device.

Here input voltage V_i and output current I_o are the dependent variables.

Input current I_i and output voltage V_o are Independent variables.

$$V_i = f_1(I_i, V_o)$$

$$I_o = f_2(I_i, V_o)$$

This can be written in the equation form as follows

$$V_i = h_{11} I_i + h_{12} V_o$$

$$I_o = h_{21} I_i + h_{22} V_o$$

The above equation can also be written using alphabetic Notations

BJT AMPLIFIERS

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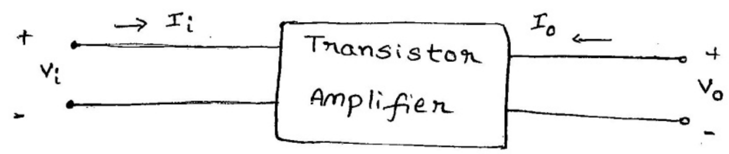

Here I_i = Input current to the Amplifier

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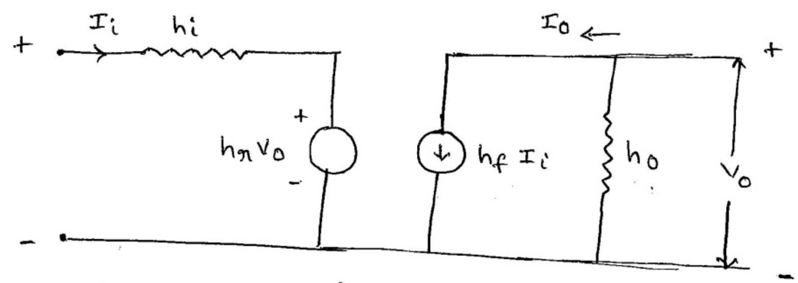
The above equation can also be written using alphabetic Notations

Based on above two equations the equivalent circuit or Hybrid Model for transistor can be drawn.



Advantages (or) Benifits of h-parameters

1) Real numbers at audio frequencies
2) Easy to measure
3) Can be obtained from the transistor static characteristic curves.
4) convinient to use in circuit analysis and design.
5) Easily convertable from one configuration to other
6) Most of the transistor manufacturers sepecify the h-parameters.

H parameter Model for CE Configuration

Let us consider the common emitter configuration shown in figure below. The Variables I_b, I_c, V_b and V_c represent total instantaneous corrents and Voltages.

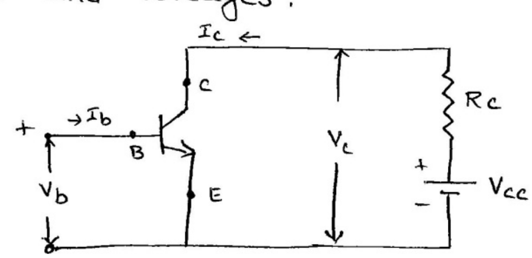
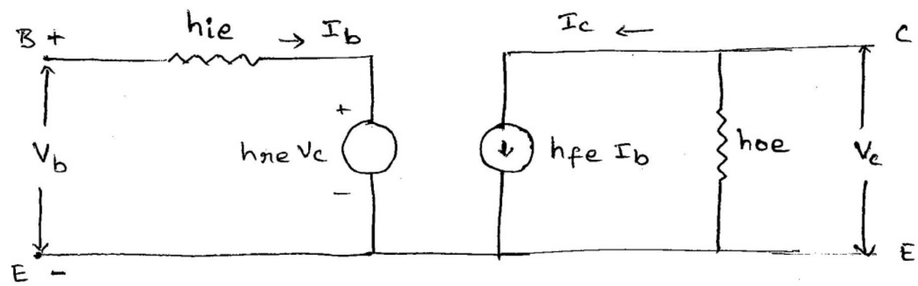


Fig: simple common emitter configuration

Here I_b - Input current V_b - Input voltage

I_c - output current V_c - output voltage

h- parameter model for common emitter configuration is shown in figure below.



$$V_b = h_{ie} I_b + h_{re} V_c$$

$$I_c = h_{fe} I_b + h_{oe} V_c$$

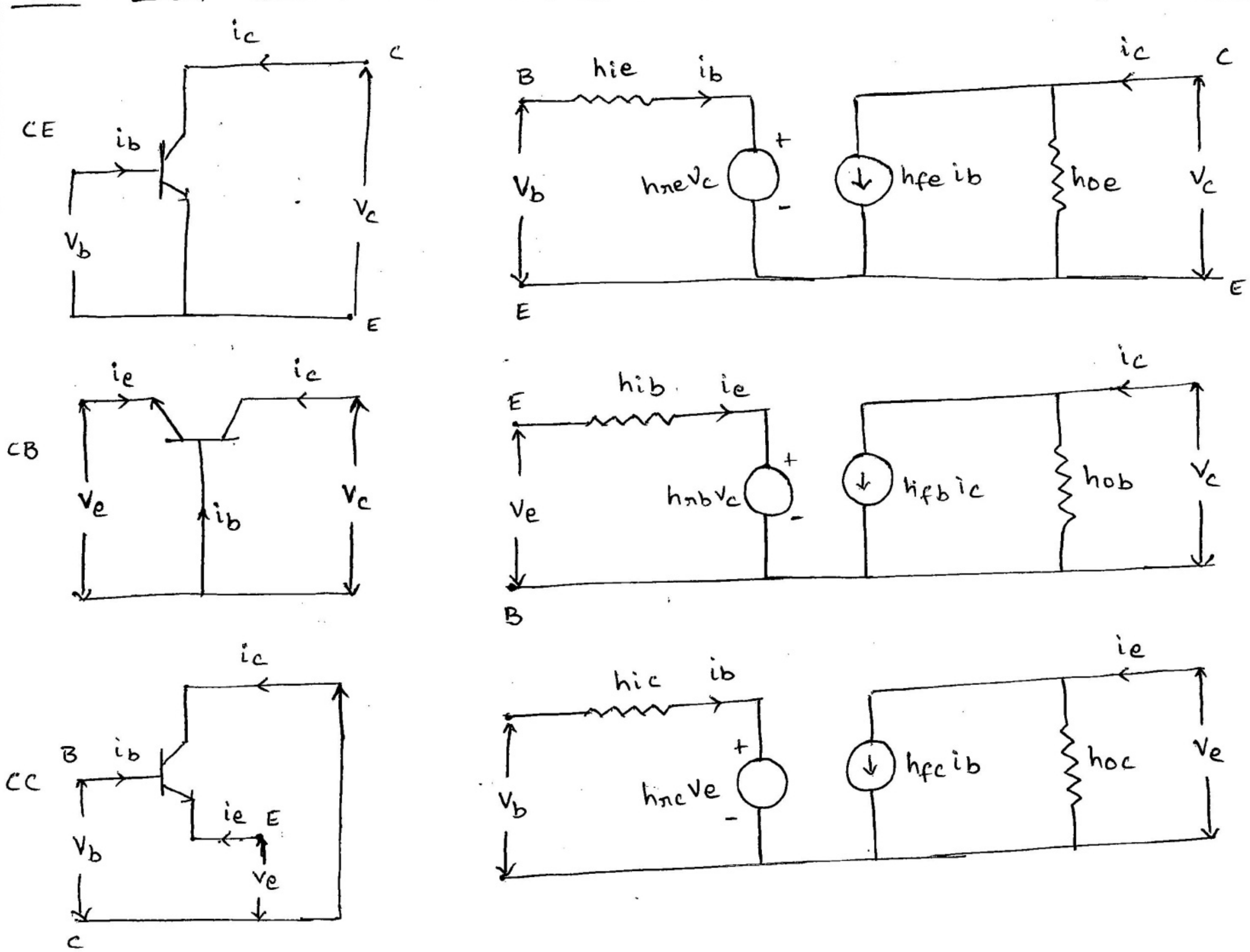
where
$$h_{ie} = \left.\frac{\Delta V_B}{\Delta I_B}\right|_{V_c = \text{constant}} = \left.\frac{V_b}{I_b}\right|_{V_c = \text{constant}}$$

$$h_{re} = \left.\frac{\Delta V_B}{\Delta V_c}\right|_{I_B = \text{constant}} = \left.\frac{V_b}{V_c}\right|_{I_b = \text{constant}}$$

$$h_{fe} = \left.\frac{\Delta I_c}{\Delta I_B}\right|_{V_c = \text{Constant}} = \left.\frac{i_c}{i_b}\right|_{V_c = \text{Constant}}$$

$$h_{oe} = \left.\frac{\Delta I_c}{\Delta V_c}\right|_{I_B = \text{constant}} = \left.\frac{i_c}{v_c}\right|_{i_b = \text{constant}}$$

Hybrid model for the transistor in three different configurations



$V_b = h_{ie} i_b + h_{re} v_c$

$i_c = h_{fe} i_b + h_{oe} v_c$

$V_e = h_{ib} i_e + h_{rb} v_c$

$i_c = h_{fb} i_e + h_{ob} v_c$

$V_b = h_{ic} i_b + h_{rc} V_e$

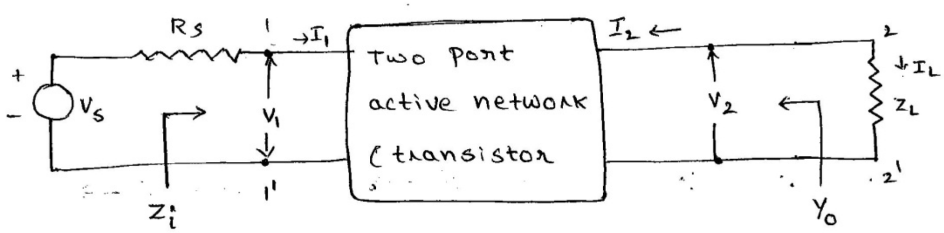
$i_e = h_{fc} i_b + h_{oc} v_e$

Typical h-parameter values for a transistor

Parameter	CE	CC	CB
h_i	1100Ω	1100Ω	22Ω
h_r	2.5×10^{-4}	1	3×10^{-4}
h_f	50	-51	-0.98
h_o	$25\,\mu A/V$	$25\,\mu A/V$	$0.49\,\mu A/V$

Analysis of a transistor amplifier circuit using h-parameter model.

A transistor amplifier can be constructed by connecting an external load and signal source as indicated in figure below. and biasing the transistor properly.



The hybrid parameter model for above network is shown in figure below.

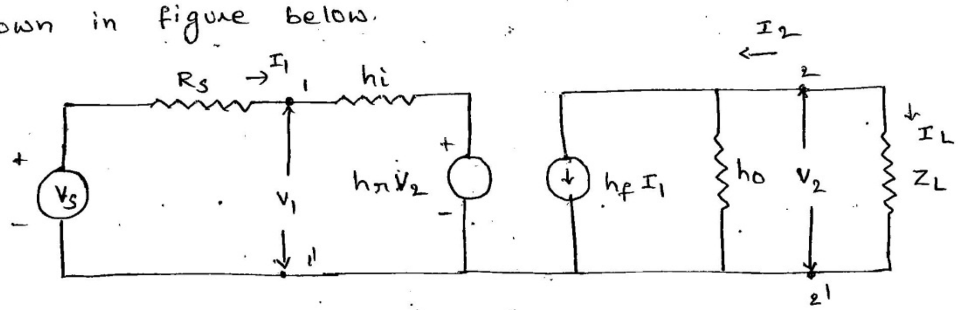


Fig: Transistor hybrid parameter model.

1) Current Gain (or) Current Amplification A_i :

For a transistor amplifier the current gain A_I is defined as the ratio of output current to input current.

$$A_I = \frac{I_L}{I_1} = \frac{-I_2}{I_1}$$

From the circuit $I_2 = h_f I_1 + h_o V_2 \longrightarrow ①$

$$V_2 = I_L Z_L = -I_2 Z_L \longrightarrow ②$$

sub ② in ①

$$I_2 = h_f I_1 - I_2 Z_L h_o$$

$$I_2 + I_2 Z_L h_o = h_f I_1$$

$$I_2 \left(1 + Z_L h_o \right) = h_f I_1 \Rightarrow \frac{I_2}{I_1} = \frac{h_f}{1 + Z_L h_o}$$

$$\boxed{A_I = \frac{-I_2}{I_1} = \frac{-h_f}{1 + Z_L h_o}}$$

	CE	CB	CC
A_I	$\frac{-h_{fe}}{1+Z_L h_{oe}}$	$\frac{-h_{fb}}{1+Z_L h_{ob}}$	$\frac{-h_{fc}}{1+Z_L h_{oc}}$

2) Input Impedance Z_i

In the circuit R_s is the signal source resistance the impedance seen when looking in to the amplifier terminals $(1, 1')$ is the amplifier input impedance Z_i

$$Z_i = \frac{V_1}{I_1}$$

From figure $V_1 = h_i I_1 + h_r V_2$

So $Z_i = \dfrac{h_i I_1 + h_r V_2}{I_1} = h_i + h_r \dfrac{V_2}{I_1} \longrightarrow (1)$

$V_2 = -I_2 Z_L = A_I I_1 Z_L$ $\left[\because A_I = \dfrac{-I_2}{I_1}\right]$

$(1) \Rightarrow Z_i = h_i + h_r \dfrac{A_I I_1 Z_L}{I_1}$

$Z_i = h_i + h_r A_I Z_L$

$Z_i = h_i - h_r Z_L \dfrac{h_f}{1 + h_o Z_L}$ $\left[\because A_I = \dfrac{-h_f}{1 + h_o Z_L}\right]$

$Z_i = h_i - \dfrac{h_f h_r}{\frac{1}{Z_L} + h_o}$

$Z_i = h_i - \dfrac{h_f h_r}{Y_L + h_o}$ $\left[\because Y_L = \dfrac{1}{Z_L}\right]$

	CE	CB	CC
Z_i	$h_{ie} - \dfrac{h_{fe} h_{re}}{Y_L + h_{oe}}$	$h_{ib} - \dfrac{h_{fb} h_{rb}}{Y_L + h_{ob}}$	$h_{ic} - \dfrac{h_{fc} h_{rc}}{Y_L + h_{oc}}$

3) Voltage gain (A_V):

The ratio of output voltage V_2 to input voltage gives the voltage gain of the transistor

$$A_V = \frac{V_2}{V_1}$$

Substituting $V_2 = -I_2 Z_L = A_I I_1 Z_L$

$$\Rightarrow A_V = \frac{A_I I_1 Z_L}{V_1} = \frac{A_I Z_L}{V_1 / I_1} = \frac{A_I Z_L}{Z_i}$$

	CE	CB	CC
A_V	$\dfrac{A_I Z_L}{Z_i}$	$\dfrac{A_I Z_L}{Z_i}$	$\dfrac{A_I Z_L}{Z_i}$

4) **Output Admittance (Y_0) :**

$$Y_0 = \frac{I_2}{V_2} \quad \text{with} \quad V_s = 0 \quad \text{and} \quad R_L = \infty$$

From the circuit $I_2 = h_f I_1 + h_o V_2$

Dividing by V_2, $\dfrac{I_2}{V_2} = h_f \dfrac{I_1}{V_2} + h_o \longrightarrow (1)$

With $V_s = 0$, by KVL in input circuit

$$R_s I_1 + h_i I_1 + h_r V_2 = 0$$

$$I_1 (R_s + h_i) + h_r V_2 = 0$$

Hence $\dfrac{I_1}{V_2} = \dfrac{-h_r}{R_s + h_i}$

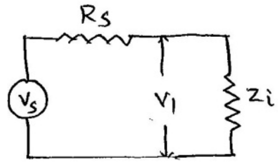
Now Eq (1) $\Rightarrow \dfrac{I_2}{V_2} = \dfrac{-h_f h_r}{R_s + h_i} + h_o$

$$\Rightarrow Y_0 = h_o - \frac{h_f h_r}{R_s + h_i}$$

	CE	CB	CC
Y_0	$h_{oe} - \dfrac{h_{fe} h_{re}}{R_s + h_{ie}}$	$h_{ob} - \dfrac{h_{fb} h_{rb}}{R_s + h_{ib}}$	$h_{oc} - \dfrac{h_{fc} h_{rc}}{R_s + h_{ic}}$

5) **Voltage gain (A_{vs}) (Including source) :**

$$A_{vs} = \frac{V_2}{V_s} = \frac{V_2}{V_1} \frac{V_1}{V_s} \Rightarrow A_{vs} = A_v \frac{V_1}{V_s}$$



$$V_1 = \frac{V_s Z_i}{R_s + Z_i} \Rightarrow \frac{V_1}{V_s} = \frac{Z_i}{R_s + Z_i}$$

Now $A_{vs} = \dfrac{A_v Z_i}{R_s + Z_i}$

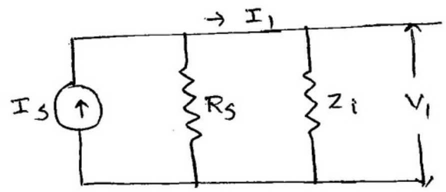
$$A_{VS} = \frac{A_I R_L}{Z_i} \times \frac{Z_i}{R_S + Z_i} = \frac{A_I R_L}{R_S + Z_i}$$

If $R_S = 0$ then $A_{VS} = \frac{A_I R_L}{Z_i} = A_V$.

6) <u>Current Amplification</u> (A_{IS})

$$A_{IS} = \frac{-I_2}{I_S} = \frac{-I_2}{I_1} \cdot \frac{I_1}{I_S} = A_I \frac{I_1}{I_S}$$

The modified input circuit using Norton's equivalent circuit for the source for the calculation of A_{IS}



$$A_{IS} = A_I \frac{R_S}{R_S + Z_i}$$

$$A_{VS} = \frac{A_{IS} Z_L}{R_S}$$

⇒ <u>In CE configuration</u>

Current Gain $A_I = \frac{-h_{fe}}{1 + h_{oe} Z_L}$ $\quad [Z_L = R_L]$

Input Impedance $Z_i = h_{ie} - \frac{h_{fe} h_{re}}{Y_L + h_{oe}}$ $\quad [Y_L = \frac{1}{Z_L} = \frac{1}{R_L}$

Voltage Gain $A_V = A_I \frac{Z_L}{Z_i}$

Output Admittance $Y_o = h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} + R_S}$

⇒ <u>In CB configuration</u>

Current gain $A_I = \frac{-h_{fb}}{1 + h_{ob} Z_L}$

Input Impedance $Z_i = h_{ib} - \frac{h_{fb} h_{rb}}{Y_L + h_{ob}}$

Voltage gain $A_V = A_I \frac{Z_L}{Z_i}$

Output Admittance $Y_o = h_{ob} - \frac{h_{fb} h_{rb}}{h_{ib} + R_S}$

⇒ In CC configuration

Current gain $A_I = \dfrac{-h_{fc}}{1 + h_{oc} Z_L}$

Input Impedance $Z_i = h_{ic} - \dfrac{h_{fc} h_{rc}}{Y_L + h_{oc}}$

Voltage gain $A_V = \dfrac{A_I Z_L}{Z_i}$

Output Admittance $Y_o = h_{oc} - \dfrac{h_{fc} h_{rc}}{h_{ic} + R_s}$

Conversion formulae for hybrid parameters

CB	CC
$h_{ib} = \dfrac{h_{ie}}{1 + h_{fe}}$	$h_{ic} = h_{ie}$
$h_{rb} = \dfrac{h_{ie} h_{oe}}{1 + h_{fe}} - h_{re}$	$h_{rc} = 1$
$h_{fb} = \dfrac{-h_{fe}}{1 + h_{fe}}$	$h_{fc} = -(1 + h_{fe})$
$h_{ob} = \dfrac{h_{oe}}{1 + h_{fe}}$	$h_{oc} = h_{oe}$

1) Characteristics of Common emitter Amplifier

1) Current gain A_I is high for $R_L < 10K\Omega$

2) The voltage gain is high for normal values of Load resistance R_L

3) The input resistance R_i is medium

4) The output resistance R_o is moderately high

Applications of common emitter amplifier :

1. of the three configurations CE amplifier alone is capable of providing both voltage gain and current gain.
2. The output resistance R_o and input resistance R_i are moderately high
3. CE amplifier is widely used for Amplification purpose

2) ## Characteristics of Common Base Amplifier :

1. Current gain is less than unity and its magnitude decreases with the increase of load resistance R_L
2. Voltage gain A_v is high for normal values of R_L
3. The input resistance R_i is the lowest of all the three configurations.
4. The output resistance R_o is the highest of all the three configurations.

Applications of common base Amplifier

The CB Amplifier is not commonly used for Amplification purpose. It is used for

1) Matching a very low impedance source.
2) As a non inverting amplifier with voltage gain exceeding unity
3) For driving a high impedance load
4) As a constant current source.

3) ## Characteristics of common collector Amplifier

1. For low value of R_L ($< 10k\Omega$) the current gain A_I is high and almost equal to that of a CE amplifier

2. The voltage gain A_V is less than unity.

3. The input resistance is the highest of all the three configurations.

4. The output resistance is the lowest of all the three configurations.

Applications of common collector Amplifier:

1. The CC Amplifier is widely used as a buffer stage between a high impedance source and low impedance load. (CC Amplifier is called emitter follower)

Comparison of Transistor Amplifier configurations.

The characteristics of three configurations are summarized in table below. Here the quantities A_I, A_V, R_i, R_o and A_p (Power gain) are calculated for $R_L = R_S = 3\,k\Omega$

Quantity	CB	CC	CE
A_I	0.98	47.5	-46.5
A_V	131	0.989	-131
A_p	128.38	46.98	6091.5
R_i	22.6 Ω	144 kΩ	1065 Ω
R_o	1.72 MΩ	80.5 Ω	45.5 kΩ

Simplified CE Hybrid model (or) Approximate CE Hybrid model (Approximate Analysis):

As the h parameters themselves vary widely for the same type of transistor, It is justified to make approximations and simplify the expressions for A_I, A_V, A_P, R_i and R_O.

The behaviour of the transistor circuit can be obtained by using the simplified hybrid model. The h-parameter equivalent circuit of the transistor in the CE configuration is shown in figure below.

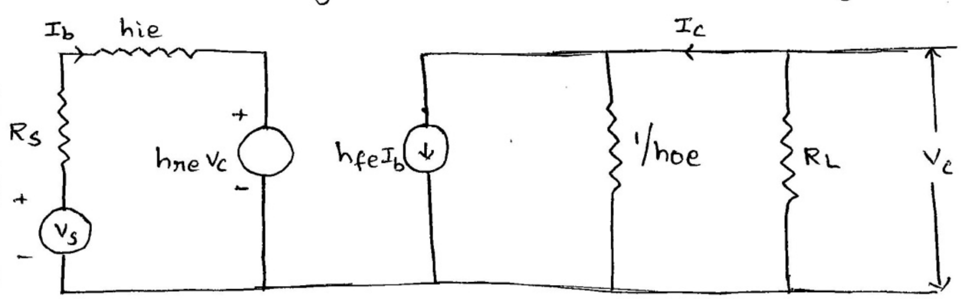


Fig: Exact CE Hybrid model.

Here $\frac{1}{h_{oe}}$ is in parallel with R_L

The parallel combination of two onequal impedances is approximately equal to the lower value ie R_L. Hence if $\frac{1}{h_{oe}} >> R_L$, then the term hoe may be neglected provided that $h_{oe} R_L << 1$

If hoe is omitted, the collector current I_c is given by $I_c = h_{fe} I_b$.

under this condition the magnitude of voltage generated in the emitter circuit is

$$h_{re}\,|V_c| = h_{re}\, I_c R_L = h_{re}\, h_{fe}\, I_b R_L$$

since $h_{re} h_{fe} \approx 0.01$, this voltage may be neglected in comparison with the voltage drop across hie. ie $h_{ie} I_b$ provided that R_L is not too large. ie if the load resistance R_L is small it is possible to neglect the parameter h_{re} and h_{oe} and the approximate equivalent circuit is obtained as shown in figure below.

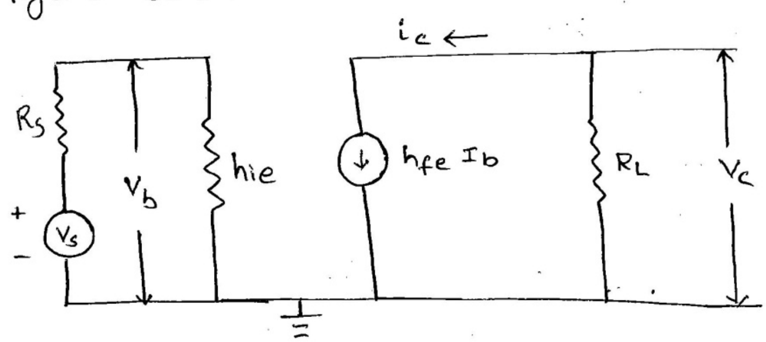


Fig: Approximate CE Hybrid model.

1) Current Gain (A_I):

The current gain for CE configuration is

$$A_I = \frac{-h_{fe}}{1 + h_{oe} R_L}, \quad \text{if } h_{oe} R_L < 0.1$$

$$\boxed{A_I = -h_{fe}}$$

2) Input Impedance (Z_i):

By exact analysis $Z_i = R_i = \dfrac{V_1}{I_1}$

$V_1 = h_{ie} I_1 + h_{re} V_2$

$$Z_i = \frac{h_{ie} I_1 + h_{re} V_2}{I_1} = h_{ie} + h_{re} \frac{V_2}{I_1}$$

$$V_2 = -I_2 Z_L = -I_2 R_L = A_I I_1 R_L \qquad \left[\because A_I = \frac{-I_2}{I_1}\right]$$

$$\Rightarrow Z_i = h_{ie} + \frac{h_{re} A_I I_1 R_L}{I_1} \qquad \left[\because V_2 = A_I I_1 R_L\right]$$

$$R_i = \left[h_{ie} + h_{re} A_I R_L\right]$$

$$R_i = h_{ie}\left[1 + \frac{h_{re} A_I R_L}{h_{ie}}\right]$$

$$R_i = h_{ie}\left[1 + \frac{h_{re} A_I R_L}{h_{ie}} \times \frac{h_{fe} h_{oe}}{h_{fe} h_{oe}}\right]$$

using the typical values for the h-parameters

$$\frac{h_{re} h_{fe}}{h_{ie} h_{oe}} \simeq 0.5$$

$$\Rightarrow R_i = h_{ie}\left[1 + \frac{0.5 A_I R_L h_{oe}}{h_{fe}}\right]$$

we know that $A_I = \dfrac{-h_{fe}}{1 + h_{oe} R_L}$ If $h_{oe} R_L < 0.1$

then $A_I = -h_{fe}$

$$\Rightarrow R_i = h_{ie}\left[1 - \frac{0.5 h_{fe} R_L h_{oe}}{h_{fe}}\right]$$

$$\Rightarrow R_i = h_{ie}\left[1 - 0.5 h_{oe} R_L\right]$$

If $h_{oe} R_L < 0.1$

then $\boxed{R_i \simeq h_{ie}}$ $\left[R_i = Z_i\right]$

voltage gain: $A_V = A_I \frac{R_L}{R_i} = \frac{-h_{fe} R_L}{h_{ie}}$

Output Impedance:

It is the ratio of V_c to I_c with $V_s = 0$ and R_L excluded. The simplified circuit has infinite output impedance because with $V_s = 0$ and external voltage source applied at output, it is found that $I_b = 0$ and hence $I_c = 0$

$$R_O = \frac{V_c}{I_c} = \infty \quad [\because I_c = 0]$$

Approximate analysis of CE Amplifier

current gain $A_I = -h_{fe}$

Input resistance $R_i = h_{ie}$

Voltage gain $A_V = \frac{-h_{fe} R_L}{h_{ie}}$

output resistance $R_O = \infty$

Analysis of CC Amplifier using the approximate Model:

Figure shows the equivalent circuit of CC Amplifier using the approximate model with the collector grounded, input signal applied between base and ground and load connected between emitter and ground.

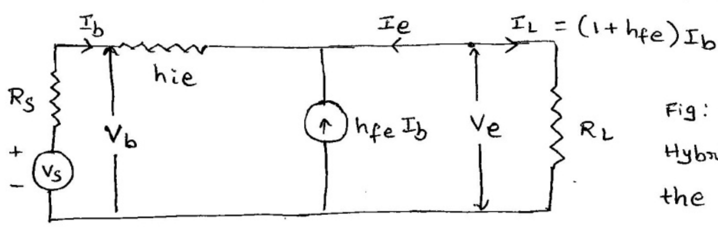


Fig: simplified Hybrid model for the cc circuit

1) current gain :-

$$A_I = \frac{I_L}{I_b} = \frac{(1+h_{fe}) I_b}{I_b} = (1+h_{fe})$$

2) Input resistance

$$V_b = I_b h_{ie} + (1+h_{fe}) I_b R_L$$

$$R_i = \frac{V_b}{I_b} = h_{ie} + (1+h_{fe}) R_L$$

3) Voltage gain

$$A_V = \frac{V_e}{V_b} = \frac{(1+h_{fe}) I_b R_L}{[h_{ie} I_b + (1+h_{fe}) I_b R_L]}$$

$$A_V = \frac{(1+h_{fe}) R_L}{h_{ie} + (1+h_{fe}) R_L} = \frac{h_{ie} + (1+h_{fe}) R_L - h_{ie}}{h_{ie} + (1+h_{fe}) R_L}$$

$$A_V = 1 - \frac{h_{ie}}{h_{ie} + (1+h_{fe}) R_L}$$

$$A_V = 1 - \frac{h_{ie}}{R_i} \quad [\because R_i = h_{ie} + (1+h_{fe}) R_L]$$

4) Output Impedance :-

output admittance ~~impedance~~ $(Y_o) = \dfrac{\text{short circuit current in o/p terminals}}{\text{open circuit voltage b/n o/p terminals}}$

short circuit current in output terminals $= (1+h_{fe}) I_b = (1+h_{fe}) \dfrac{V_s}{R_s + h_{ie}}$

open circuit voltage b/n output terminals $= V_s$

$$\therefore \quad Y_o = \frac{1+h_{fe}}{R_s + h_{ie}} \Rightarrow R_o = \frac{h_{ie} + R_s}{1 + h_{fe}}$$

output impedance including R_L ie $R_o' = R_o || R_L$

Analysis of CB Amplifier using the approximate model

Figure shows the equivalent circuit of CB amplifier using the approximate model, with the base grounded, input signal is applied between emitter and base and load connected between collector and base

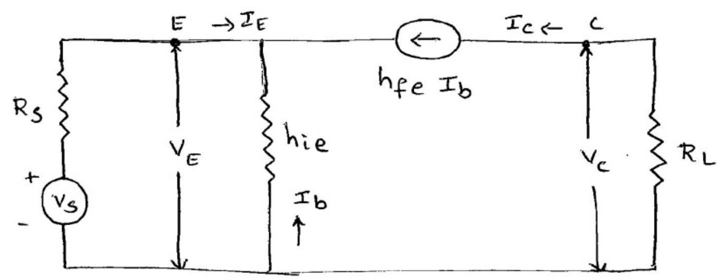


Fig: Simplified Hybrid model for the CB circuit

1) Current gain:

From the figure above $A_I = \dfrac{-I_c}{I_e} = \dfrac{-h_{fe} I_b}{I_e}$

$$I_e = -(I_b + I_c)$$

$$I_e = -(I_b + h_{fe} I_b) = -(1+h_{fe}) I_b$$

$$\therefore A_I = \frac{-h_{fe} I_b}{-(1+h_{fe}) I_b} = \frac{h_{fe}}{1+h_{fe}} = -h_{fb}$$

2) Input Resistance:

Input Resistance $R_i = \dfrac{V_e}{I_e}$

From figure $V_e = -I_b h_{ie}$, $I_e = -(1+h_{fe}) I_b$

$$R_i = \frac{h_{ie}}{1+h_{fe}} = h_{ib}$$

3) Voltage gain:

$$A_V = \frac{V_c}{V_e}$$

$$V_c = -I_c R_L = -h_{fe} I_b R_L$$

$$V_e = -I_b h_{ie}$$

$$A_V = \frac{h_{fe} R_L}{h_{ie}}$$

Output Impedance

$$R_o = \frac{V_c}{I_c} \quad \text{with} \quad V_s = 0, \quad R_L = \infty$$

with $V_s = 0$, $I_e = 0$ and $I_b = 0$ hence $I_c = 0$

$$\therefore \quad R_o = \frac{V_c}{0} = \infty$$

Approximate Analysis of CB Amplifier

1) Current gain $A_I = \dfrac{h_{fe}}{1+h_{fe}} = -h_{fb}$

2) Input Resistance $R_i = \dfrac{h_{ie}}{1+h_{fe}} = h_{ib}$

3) Voltage gain $A_V = \dfrac{h_{fe} R_L}{h_{ie}}$

4) Output Resistance $R_o = \infty$

Approximate Analysis of CC Amplifier

1) Current gain $A_I = (1+h_{fe})$

2) Input resistance $R_i = h_{ie} + (1+h_{fe}) R_L$

3) Voltage gain $A_V = 1 - \dfrac{h_{ie}}{R_i}$

4) Output Resistance $R_o = \dfrac{h_{ie} + R_s}{1+h_{fe}}$

Problem: A CE Amplifier is drawn by a voltage souce of Internal resistance $r_s = 800\Omega$ and the load impedance is a resistance $R_L = 1000\Omega$. The h parameters are $h_{ie} = 1k\Omega$, $h_{re} = 2\times10^{-4}$, $h_{fe} = 50$ and $h_{oe} = 25\mu A/V$, compute the current gain A_I, input resistance R_i, voltage gain A_V, and output resistance R_o using exact analysis and approximate analysis.

Solution: Given data

$r_s = 800\Omega$, $R_L = 1000\Omega$, $h_{ie} = 1k\Omega$, $h_{re} = 2\times10^{-4}$, $h_{fe} = 50$, and $h_{oe} = 25\mu A/V$

Exact Analysis:-

Current Gain $A_I = \dfrac{-h_{fe}}{1 + h_{oe}R_L} = -48.78$

Input Resistance $R_i = h_{ie} - \dfrac{h_{fe}h_{re}}{h_{oe} + \frac{1}{R_L}} = 990.24\Omega$

Voltage gain $A_V = A_I \dfrac{R_L}{R_i} = -49.26$

Output Resistance

$$Y_o = h_{oe} - \frac{h_{fe}h_{re}}{h_{ie} + R_s} = 194\times10^{-5} \text{ mho}$$

$$R_o = \frac{1}{Y_o} = 51.42\,k\Omega$$

Approximate Analysis:

$A_I = -h_{fe} = -50$

$R_i = h_{ie} = 1k\Omega$

$$A_V = \frac{-h_{fe} R_L}{h_{ie}} = \frac{-50 \times 1000}{1000} = -50$$

$$R_o = \infty$$

<u>Problem</u>: A voltage source of Internal resistance $R_s = 900\,\Omega$ drives a CC amplifier using load resistance $R_L = 2000\,\Omega$. The CE h-parameters are $h_{ie} = 1200\,\Omega$, $h_{re} = 2 \times 10^{-4}$, $h_{fe} = 60$ and $h_{oe} = 25\,\mu A/V$. Compute the current gain A_I, input Resistance R_i, voltage gain A_V, and output resistance R_o using exact analysis and approximate analysis.

<u>Sol</u> <u>Conversion formulae</u>:

$$h_{ic} = h_{ie} = 1200\,\Omega$$

$$h_{fc} = -(1 + h_{fe}) = -(1 + 60) = -61$$

$$h_{rc} = 1$$

$$h_{oc} = h_{oe} = 25\,\mu A/V$$

<u>Exact Analysis</u>:

$$A_I = \frac{-h_{fc}}{1 + h_{oc} R_L} = 58.095$$

$$R_i = h_{ic} - \frac{h_{fc} h_{rc}}{Y_L + h_{oe}} = 117.39\,K\Omega$$

$$A_V = \frac{A_I R_L}{R_i} = 0.9897$$

Output Admittance

$$Y_o = h_{oc} - \frac{h_{fc} h_{rc}}{h_{ic} + R_s}$$

$$\Rightarrow R_O = \frac{1}{Y_o} = 34.396\,\Omega$$

Approximate Analysis

$$A_I = 1 + h_{fe} = 1 + 60 = 61$$

$$R_i = h_{ie} + (1 + h_{fe}) R_L = 123.2\,K\Omega$$

$$A_V = 1 - \frac{h_{ie}}{R_i} = 0.99$$

$$R_o = \frac{h_{ie} + R_s}{1 + h_{fe}} = 34.43\,\Omega$$

Problem:

For a CB transistor Amplifier driven by a voltage source of internal resistance $R_s = 1200\,\Omega$, the load impedance is a resistor $R_L = 1000\,\Omega$. The h-parameters are $h_{ib} = 22\,\Omega$, $h_{rb} = 3\times10^{-4}$, $h_{fb} = -0.98$, $h_{ob} = 0.5\,\mu A/V$. Compute the current gain A_I, Input impedance R_i, voltage gain A_V, overall voltage gain A_{VS}, over all current gain A_{IS}, output impedance R_o and power gain A_p using exact and approximate analysis.

Solution:

$$\text{Current gain } A_I = \frac{-h_{fb}}{1 + h_{ob} R_L} = 0.98$$

$$\text{Input Impedance } R_i = h_{ib} - \frac{h_{fb} h_{rb}}{Y_L + h_{ob}} = 22.3\,\Omega$$

voltage gain $A_V = \frac{A_I R_L}{R_i} = \frac{0.98 \times 1000}{22.3} = 43.94$

overall voltage gain $A_{VS} = \frac{A_V R_i}{R_i + R_S} = 0.802$

overall current gain $A_{IS} = \frac{A_I R_S}{R_i + R_S} = 0.962$

output Admittance $Y_O = h_{ob} - \frac{h_{fb} h_{rb}}{h_{ib} + R_S} = 0.74 \times 10^{-6}$ mho

$$R_O = \frac{1}{Y_O} = 1.35 M\Omega$$

Power gain $A_P = A_V A_I = 43.06$

Approximate Analysis :

1) $A_I = -h_{fb} = 0.98$

2) $R_i = h_{ib} = 22\,\Omega$

3) $A_V = \frac{h_{fe} R_L}{h_{ie}}$

$A_V = \frac{49 \times 1000}{1100}$

$A_V = 44.54$

4) $R_O = \infty$

A_{VS}, A_{IS}, A_P are same as that of Exact analysis.

$\because$ conversion formulae

$h_{fb} = \frac{-h_{fe}}{1 + h_{fe}}$

$\Rightarrow h_{fe} = \frac{-h_{fb}}{1 + h_{fb}} = 49$

$h_{ib} = \frac{h_{ie}}{1 + h_{fe}}$

$\Rightarrow h_{ie} = h_{ib}(1 + h_{fe})$

$h_{ie} = 22(1 + 49) = 1100\,\Omega$

$$V_i = h_i I_i + h_r V_o$$

$$I_o = h_f I_i + h_o V_o$$

Definitions of h- parameter:

The parameters in the above equation are defined as follows

$h_{11} = h_i = \left.\frac{V_i}{I_i}\right|_{V_o = 0}$ = Input resistance with output short circuited.

$h_{12} = h_r = \left.\frac{V_i}{I_o}\right|_{I_i = 0}$ = Reverse voltage transfer ratio with input open circuited.

$h_{21} = h_f = \left.\frac{I_o}{I_i}\right|_{V_o = 0}$ = short circuit forward current gain with output short circuited.

$h_{22} = h_o = \left.\frac{I_o}{V_o}\right|_{I_i = 0}$ = output Admittance with input open circuited.

BJT H-parameter Model:

Based on the definition of hybrid parameters the mathematical model for two port networks known as h-parameter model (Hybrid Parameter model) can be developed.

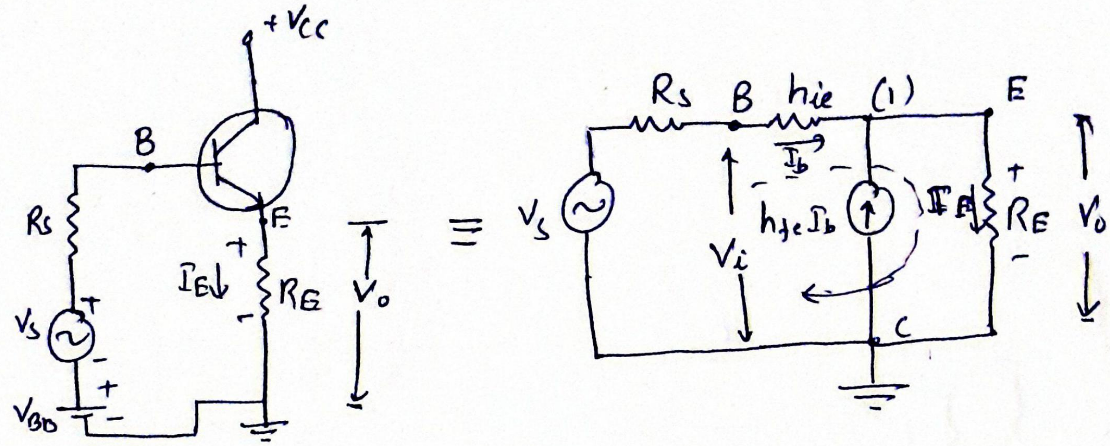
The two equations of a transistor is given by

$$V_i = h_i I_i + h_r V_o$$

$$I_o = h_f I_i + h_o V_o$$

(1)

Derivation for CC configuration



Current Gain (A_I)

Applying KCL at node (1)

$$I_E = I_B + h_{fe} I_b$$

$$= I_B(1+h_{fe})$$

$$\boxed{I_E = I_B(1+h_{fe})} \quad \text{—(1)}$$

$$A_I \text{ (Current Gain)} = \frac{I_o}{I_b} = \frac{I_E}{I_B} \qquad \{I_o = I_E\}$$

sub value of I_E from above eq

$$A_I = \frac{\cancel{I_B}(1+h_{fe})}{\cancel{I_B}}$$

$$\boxed{A_I = (1+h_{fe})}$$

Applying KVL for the outer loop:-

$$V_i = h_{ie} I_b + I_E R_E$$

Sub. value of $I_E = (1+h_{fe}) I_b$

$$V_i = h_{ie} I_b + (1+h_{fe}) I_b R_E$$

$$\boxed{V_i = I_b [h_{ie} + (1+h_{fe}) R_E]}$$

$$R_i = \frac{V_i}{I_b} = h_{ie} + (1+h_{fe}) R_E$$

$$\therefore \boxed{R_i = h_{ie} + (1+h_{fe}) R_E}$$

Voltage Gain (A_v)

From o/p loop

$$V_o = I_E R_E$$

$$= (1+h_{fe}) I_B R_E \qquad \{ I_E = (1+h_{fe}) I_B \}$$

$$V_o = (1+h_{fe}) I_B R_E$$

$$\text{Voltage Gain}(A_v) = \frac{V_o}{V_i} = \frac{(1+h_{fe}) \cancel{I_B} R_E}{\cancel{I_B} [h_{ie} + (1+h_{fe}) R_E]}$$

$$\frac{V_o}{V_i} = \frac{(1+h_{fe}) R_E}{[h_{ie} + (1+h_{fe}) R_E]}$$

dividing num. & den. by $[(1+h_{fe})R_E]$ ③

we get

$$A_V = \frac{1}{1 + \frac{h_{ie}}{(1+h_{fe})R_E}} \quad -②$$

Now,

$$R_i = (1+h_{fe})R_E + h_{ie}$$

$$R_i \cong (1+h_{fe})R_E \quad \{\text{as } h_{ie} \text{ is very small and can be neglected}\}$$

$$\therefore \quad R_E = \frac{R_i}{1+h_{fe}} \quad -③$$

sub. value of R_E in eq ②, we get

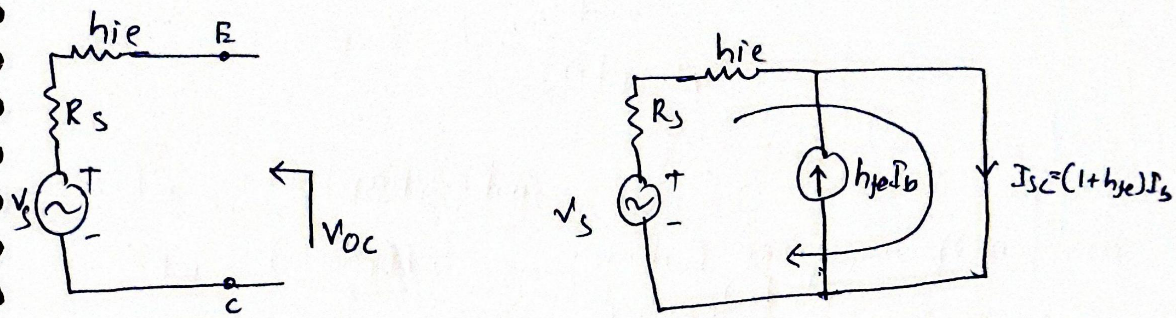
$$A_V = \frac{1}{1 + \frac{h_{ie} \cdot \cancel{(1+h_{fe})}}{\cancel{(1+h_{fe})} \cdot R_i}}$$

$$A_V = \frac{1}{\left(1+\frac{h_{ie}}{R_i}\right)}$$

$$\boxed{A_V = \left(1+\frac{h_{ie}}{R_i}\right)^{-1}}$$

O/P Resistance (R_o)

$$R_o = \frac{V_{oc}}{I_{sc}}$$



(a) Circuit for Voc

(b) Circuit for Isc

From fig (a)

$$V_{oc} = V_s \quad - (4)$$

Now from fig (b), Isc can be calculated.

Applying KVL in loop.

$$V_s = I_b R_s + h_{ie} I_b$$

$$V_s = I_b (R_s + h_{ie})$$

$$\boxed{I_b = \frac{V_s}{(R_s + h_{ie})}}$$

Short circuit current $I_{sc} = (1+h_{fe}) I_b$

$$I_{sc} = \frac{(1+h_{fe}) \cdot V_s}{(R_s + h_{ie})} \quad - (5)$$

$$\therefore \; R_o = \frac{V_{oc}}{I_{sc}} = \frac{\cancel{V_s} \cdot (R_s + h_{ie})}{(1+h_{fe}) \cdot \cancel{V_s}}$$

$$\therefore \; \boxed{R_o = \frac{(R_s + h_{ie})}{(1 + h_{fe})}}$$