

## Jaipur Engineering College & Research Centre, Jaipur

# Lecture Notes 3EE4-06: Analog Electronics ACADEMIC SESSION 2020-21

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## VISION OF ELECTRICAL ENGINEERING DEPARTMENT

Electrical Engineering Department strives to be recognized globally for outcome based knowledge and to develop human potential to practice advance technology which contribute to society.

## MISSION OF ELECTRICAL ENGINEERING DEPARTMENT

- M1. To impart quality technical knowledge to the learners to make them globally competitive Electrical Engineers.
- M2. To provide the learners ethical guidelines along with excellent academic environment for a long productive career.
- M3. To promote industry-institute relationship.



### **PROGRAM OUTCOMES**

- 1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems in Electrical Engineering.
- **2. Problem analysis:** Identify, formulate, research literature, and analyze complex engineering problems reaching substantial conclusions using first principles of mathematics, natural sciences, and engineering sciences in Electrical Engineering.
- **3. Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations using Electrical Engineering.
- **4.** Conduct investigations of complex problems: Use research based knowledge and research methods including design of experiments, analysis and interpretation of data and synthesis of the information to provide valid conclusions using Electrical Engineering.
- **5. Modern tool usage:** Create, select and apply appropriate techniques, resources, and modern engineering and EE tools including prediction and modeling to complex engineering activities with an understanding of the limitations in EE.
- 6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice using EE.
- 7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of EE and need for sustainable development in EE.
- **8.** Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice using EE.
- **9. Individual and team work:** Function effectively as an individual and as a member or leader in diverse teams, and multi-disciplinary settings in EE.
- **10. Communication:** Communicate effectively on complex engineering activities with the engineering community and society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations and give and receive clear instructions.
- **11. Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage EE projects and in multi-disciplinary environments.
- **12. Life-long learning:** Recognize the need for and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological changes needed in EE.



## **COURSE OUTCOMES:**

On successful completion of the course, the students will be able to: -

CO1	Understand the characteristics of Diodes, concepts behind the Clippers, and Clampers. Design and analysis of various rectifier and amplifier circuits
CO2	Analyze the characteristics of current flow in a bipolar junction transistor and MOSFET & different electronic devices such as Amplifiers
CO3	Understand the dynamics of Linear & Non Linear Devices



# Syllabus



#### RAJASTHAN TECHNICAL UNIVERSITY, KOTA SYLLABUS

2<sup>nd</sup> Year - III Semester: B.Tech. (Electrical Engineering)

#### **3EE4-06: Analog Electronics**

Credit: 3 3L+0T+0P

#### Max. Marks: 150 (IA:30, ETE:120) End Term Exam: 3 Hours

SN		Hours
1.	Diode circuits	
	P-N junction diode, I-V characteristics of a diode; review of half-	A
	wave and full-wave rectifiers, Zener diodes, clamping and clipping	
	circuits.	
2.	BJT circuits	
	Structure and I-V characteristics of a BJT; BJT as a switch. BJT	
	as an amplitier: small-signal model, biasing circuits, current	8
	mirror; common-emitter, common-base and common collector	
	ampiners; Smail signal equivalent circuits, high-frequency	
-	MOSEET circuits	
<b>.</b>	MOSFET structure and LV characteristics. MOSFET as a switch	
	MOSFET as an amplifier: small-signal model and biasing circuits.	
	common-source, common-gate and common-drain amplifiers;	8
	small signal equivalent circuits - gain, input and output	
	impedances, transconductance, high frequency equivalent circuit.	
4.	Differential, multi-stage and operational amplifiers	
	Differential amplifier; power amplifier; direct coupled multi-stage	
	amplifier; internal structure of an operational amplifier, ideal op-	8
	amp, non-idealities in an op-amp (Output offset voltage, input bias	
	current, input offset current, slew rate, gain bandwidth product)	
а.	Idealized analysis of on amp circuits. Investing and the investing	
	amplifier differential amplifier instrumentation amplifier	
	integrator active filter P PI and PID controllers and lead/lag	8
	compensator using an op-amp, voltage regulator, oscillators (Wein	
	bridge and phase shift).	
	Analog to Digital Conversion.	
6.	Nonlinear applications of op-amp	
	Hysteretic Comparator, Zero Crossing Detector, Square-wave and	6
	triangular-wave generators, Precision rectifier, peak detector.	
	Monoshot	
1	TOTAL	

Office of Dean Academic Affairs Rajasthan Technical University, Kota



Unit: 1

**Chapter: Diode Circuits** 



DATE Unit-1 9 P-N. Junction Diodes 3 3 introduction to semiconductors Basic Semiconductors are a special class of elements having a conductivity between that of a good conducta and that of an insulator 6 0 Single-Cuystal Sens conducter 9 It can be pure as silicon or germa compounds such as gallium avisenide (admiun 0 compound semiconductor Selenide 0 9 Most care only frequently used are bre, Si, and GaAs. 9 Insulator - Material that does not conduct electrical 0 avocent. eg. paper, plastic, rubber etc 0 9 Conductor -: Material or substances which allow 9 electricity to flow through them. eg > coppers etc. Energy Levels - Eg = 0.67 ev (Ge); Eg = 1.1ev (Si); Eg-1.43ev Every Energy Energy CB C-B Unable 6 0 Bando CB Eg 25ev 19 to seeuch Ollehat 0 0 VB conduction level VB Valence e bound Conductor Semiconductor Insulator to the alouve twee



6 2 C 07 Semiconductor Types -07 T Semiconductor T 0 Intrinsic Exterinsic 7 C-**S** P-Type N-Type C 0 0-Interinsic Semiconductor-0-A pure form of Semiconductors 0 \* Conduction is either due to thermal excitation or 0 crystal defects example Si, Ge, CraAs (Gallium Arsently) 0 \* Number of holes is equal to number of face electron 0 0 Extruinsic Semiconductor -0 A semiconductor doped by a 0 Specific impurity which is able to deeply modify its electrical properties, making it suitable for electronic 0 0 applications ( diade, an transistors etc) or optoelectronic 0 applications (light emitters and detectors). a <u>N-Type Semiconductor</u> <u>The the added impurity is a</u> <u>pentavalent atom then the resultant semiconductor is</u> <u>N-type Semiconductor eg: Phosphorus, Ansenic</u> <u>Bismuth, Antimony etc.</u> 2 0 0 2 0



0 3 9 \$ P-type Semiconductor touvalent atom then the resultant semiconductor is called P-type Semiconductor. example -: Bogon, Gallium, 6 6 9 0 indrum étc. 6 -N-type & P-type---0 -G -0 2 F E G De Ð G 0 6 Θ 0 -Ð 1 0 6 Ð 2 0 Θ Θ 0 plujosity cusoiers (hules! Hinogeity Seepresenter O Seepresenter O Seepresenter O Seepresenter O O currens gab. by ( e (me 0 0 60 douon (F) e G 0 OG G · (7) ions 0 (7) · 6. Θ - Accepton Do eD °Q 0 .0 0 Θ lows Majority Curviers e- (Minosuly Ponos ions 5 6 6 6 6 6 6 6 6 6 6 6 (usivers) (electron) N-Kype. P-type LE DEPAKIMENT rage y



6 4 0 Semiconductor Diode (P-N Junction) diod -0 Construction When a P-type material is Joined with an N-type material by using doping techingue. A Junction is formed and is of Called P-N Junction diade. N-type material has high concentrator The washing high concenteration of holes. Hence at the junction or there is a tendency of free electrons to diffuse over to the P-side and holes to the N side. This process is 0 0 called diffusion. 0-Junction. meterlic contac! 0-0 0 (An ode (A) Cathode (K) 0 Q O. Symbol Q. conventional Covert flow. 0 0 0 Working of Diode -9 The working of clipcle is divided into a 3 types Q Q (D No Applied Bias (V=OV) Q 3 Reverse Blas Condition (Vo< ov) Q Q 3) Forward Bias Condition (Vp>ov) I age I



DATE ( No Applied Bias (V=OV) Depletion Region Minosuly (cooriers Hetal contact Hujosuity 0000 Θ ο Θ 6000 tarriers 0°-6 (F) DODO GGDD Ð Ð 0 0 01 Ð Io2 Omt Ip = OmA + V0=0V -NoBias a) Internal Disteribution (Ondition) Vo=OV (noBias) col charg 6) Diode Symbol with the. D defined polarity and In=OmA the current direction From the above figure, when the two materials are joined and holes in the sugion of the junction will the electron combine which sesults the lack of free carriers the junction. The accumulation of charge carriers near the junction (ie regative ions on P-side and positive ions On n side) forms depletion region due to the depletion of free carriers in the region. For No-Bias condition, no external voltage is applied ie V = OV and the cuovent (mayority) is also zero. But



Biasing - The setting of initial operating conditions ( worked and voltage ) of an active device. is an amplifies 0 For the case of no-bias condition, minority coveriers (holes) in n-region lends to move toward the P-side and starts accumulating at the junction Same will happen on p-region Now when we consider majority carriers (e-) for n-type have to overcome the altractive force. of the layer of +ve ions in the n-type and vicevers Hence for NoBias condition we can conclu that the net flow of charge in one direction Zeru-2 Reverse Bias Condition (Vp < OV) (OFFstate when an external potential is applied across the P-N Junction in such a way that the terminal is connected to n-type and negative terminal is connected to P-type as shown Is (Mnosity woven flow) Imajority = OA-> 1 -00 + O n Depletion Region -+++++ Reverse Biased P-N VD Junetion EE DEPARTMENT Page 12



Biasing : Biasing is referred to a fixed DC voltage or \_\_\_\_\_ convent applied to a terminal of an electronic component such that a proper operating condition cambrobking 0 The number of anonecount the ions in the across the Lepletion region (near n-lype) will start increase (dame is the case with the ions near p-type region) due to the attractive forces across the positives negative potential due to the applied voltage --Due to which the thickness of depletion layer increases due to which the potential barrier across -0 the junction increases and as a result it become difficult for majority carriers to overcome it. Hence, the majority carriers unrent for this reverse biased becomes zero. However, the minority Charge curviers can easily flow through this potential barrier and a minority current (UA) always flow deving Deverse biased Condition The avocent & which exists under surverse bias conditions is called the scenerse saturation current (Is) → 3 Forward Bias condition (Vp >OV) (ON state) When a +ve voltage is applied across the diode in Such a way that the +ve terminal is connected to 6666 P-type and -ve terminal is connected to N-type On applying a +ve potential, due to recombination the +ve and -ve ions across the depletion layer will start getting elecompine and as a result the depletion **EE DEPARTMENT** Page 13



layer will start reducing reducing and after a time period it will diminish completely. As a result their is a large flow of majority charge is caroviers across the junction. Due to this the majority charge is current start flowing and the device is turned in the start flowing and the device is turned in the start flowing and the device is turned in the start flowing and the device is turned in the start flowing and the device is turned in the start flowing and the device is turned in the start flowing and the device is turned in the start flowing and the device is turned in the start flowing and the device is turned in the start flowing and the device is turned in the start flowing and the device is turned in the start flow in the start fl on Current Equation e VolnVr (For forward Big) ID = Is e VD/NVT (Fon the value Is - reverse saturation account. Vp - Applied forward - bias Voltage across the diade. C n - ideality factor (n=1) C VI - Thesmal voltage on Threeshold Voltage C C VI = KTK K- Boltzmann's Constand C = 1.38×10-23 J/10 9 C Tu -> Absolute Temp. 6 9 -> magnitude ob e-16×10-19 C. 5 5 Io -- Is ( e Vo/ny 5 (For reverse Bias) 6 To - - Is Vois-ve ID = Js (e -1) = Js (1-1) = OmA Vo= 0



Q-point - (operating point of a derrice). V-I characteristics (mA) Forward stand stange. avocent +' 1 Forward Knee Bias Voltage Reverse +V Forward Vollage -SomA 0.3 v (Germanium Cresmanin Ort V (silicon) -20 mAsilica Reverse Bias Reverse (Practical Curve) -T(MA) Curvent Toleal Diocle-T Adrode which acts as a perfect conductor When a forward > v biased vallage is applied and acts as an insultator when a sueverse valtage is 1-1 applied. OCOnstatic Resistance : Ro = Vo ID Dyananic Resistance on -ASC. AVe DIO



PAGE NO. : 10 \* Rectification -Parocess of converting a.c. voltage into d-C. Voltage 0 It is achieved with T 🐋 1) step = down Transformer 2) Rectifier 1-3) Filter 4) Voltage regulation circuits -230V AC Rgy Transformer Rectifier Smoothing Regulator Mair 5va -0 Block Diagram of a Regulated Power Supply System. Transformer - Step down 2300 AC mains to low Voltage Ac Rectifier → convert AC to DC, but with varying ~ i.e f ≠ 0.
Smoothing → Smooth the DC forom varying greatly.
In Small - supple. Regulator -> Eliminates supple by setting DC 0/P 10a fixed voltage.



2 Rec Filier -A device which offers a low elesistance C the current is one direction but a high Istance to the current in opposite direction. 6 resistance to 0 · converte sinusodial i/ waveform to uniderectional 6 0 Waveform C → A rectifier is a derrice which converts a.c. voltage to pulsating dc voltage. C Characteristics of Rectifier Circuit-1) Average on DC current-Area of one cycle of curve divided by the base. Avg. Value / DC / Mean Value = Area over one period Total Time period Vy (wt) Vdcz + @ Effective or RMS cuovent function of time is given by area of one cycle of the curve which represent square of function divide by the base.



12  $V_{grms} = \int_{T}^{T} V_{a}^{2}(\omega t)$ B Peak Factor -Ratio of Peak value to sims value Peak Factor G Form Factor-Ratic Form Factor G Ripple Factor (T)-: to the dc compone T= Vac Vac 2 Vame Peak Factor = Peak Value Sims Value Ratio of RMS Value to Average Value Form Factor = RMS Value Average Value. to the dc component in the OfP. T= Vac Vdc Vac 2 Vams - Vac



PAGE NO. : 13 DATE : 6 Efficiency - (n) Ratio of d.C. of Power to AC if Power O/P Power N= I/p Power Peak Inverse Voltage (PIV)that a diode can withstand without destroying Itage the junction 8 Transformer Utilization Factor (OIF) D. C power to be delivered to the load in a sectifies circuit decides the grating of the transformer used in circuit TUF = Pdc 9) of Regulation-Voribtion of d.c. - of rullage as a function of of d.c. load avocent. Parloated) 1/ Regulation = VNL - VFL × 100 VFL 0 **EE DEPARTMENT** Page 19



DATE : 3 For an ideal power supply, %. Regulation is Zero. Ŝ 5 3 Classification -3 1) Half - Wave Rectifier 2) Full - Wave Rectifier 3) Bridge Rectifier Talf Wave Rectifier: Converts a.c. Voltage into a pulsation Voltage using only one half cycle of the applied a.c. Voltage. 3 Pulsating PCO/P Voltage AC R, ip Vi Constructionusing step-down bransformer. Let V= Vm Sin(wt) where Vm is peak value of secondary nr. Vallan.



12 Operation-For the half cycle when a +ve half cycle of i/p o.c tage is applied. The diode Dis forward biased. hich is replaced by S. C) and starts conducting. e current starts flowing through the circuit a voltage drop (Vi) appear across R. Let (Va) is the ofp voltage then  $V_0 = V_{\mu}$ Ć FB D-S.C C VLD C C C C No Opeq. Vo=Vi C 0 0 Applying KVL in the off loop 7/2 0 0 C V1-DE = 0 Q 0 VL= Vi 0 Applying leve in the OP loop G **EE DEPARTMENT** Page 21



0 3 Vo= VL 0 5 for forward biased case. Va = Vi T 0 -For -ve half cycle 1 p (seplaced by o.C) 1 --Vi. -V.R. V c 0 For the case of -ve half cycle diade D is reversed biased and is suplaced by open circuit Hence the current flowing through the circuit is zero and hen the off obtained is zero. 0 -Vo + Th T 0 Vo 0 0 0 1 0 RL Vo=OV 0 1 -Vm 10 0 40 T 40 100 Vo=V=OV :: I=0 VL= IR, = OV rage 22 EE DEPARTMENT



U D Average Voltage: Vdc= + [Vd(art) C w=27) C Let wt = 0 C O W-sconstand dt = do C 6=0 6= TA Tezto 217 B=0 B=211 C Vdc 2 Viel(0) Vd = Vi C T=217 C 20 0 Vm Sinto) dB. C 2TT on solving. 0 0 Vm x2 0 211 Vdc 2 Vm C 0 . 0 @ Average current: 0 1 0 Ide = Im 0 0 3 RMS Voltage -0 G. Vorms 2  $V^2 d(\omega t)$ ..... 9 (Vm Sin(wt) d (wt) -999 Vams 2 Vm



PAGE NO : 18 DATE : 1 1
V RMS Curvent Toms 2 Tm T
S Peak Facture
= <u>Peak Value</u> Ims Value
$= \frac{Vm}{Vm/2}$
Peak Factor = 2
= <u>RMS Value</u> avg. Value
$\frac{Vm/2}{\sqrt{m/n}} = \frac{Tm/2}{\sqrt{m/n}}$
Form Factor = $1.57$
Factor: T= Vac Vac Vac = Virms - Vac
$\frac{1}{2} = \frac{Vains - Vac}{Vac} = \frac{Vains - 1}{Vac} = \frac{1 \cdot 21}{Vac}$ $\frac{Vac}{Vac} = \frac{Vains - 1}{Vac} = \frac{1 \cdot 21}{Vac}$



PAGE NU. 19 (8) Efficiency (n) 6/P Power \* 100 Nz ilp Power 40.8% Pac + 100 9 TUF -TUF = Pac Packnated) TUF = 0.286 entral As IUF is low it shows that half wave circuit, transformer is not fully utilized. ( PIV-Haximum reverse vallage that a diode can withstand without destroying the Junction. PIV = Vm Disadvantages ) Ripple factor is high. ) Efficiency is low ) TUP is low



PAGE NO : 0 20 DATE 0 Full Wave Rechfies-Converts an ac voltage into a 1 pulsating dc voltage using both half cycles of the applied 0 ac voltage 0 Two diodes are connected in the circuit through load Re by using a center - tap transformer. a common Center - tap transformer -0 It produces two sinusoidal 0 same magnitude and frequency but Waveforms the secondary. out of phase w.r.t to the ground in winding of the transformer 0 1 Vin 1 Vm î 27 G 0 0 R 11 -0 Vin R, 11 1, -12 -A 210 C U 0 🌑 Vi Dz ٠ II Working-For +ve half cycle 5 5 when a +ve half sly is applied across the slp. The 0 diode D, is forward biased a while Piode D, is -0 reverse biased due to which diode P, starts conducting -0 while D, is acting as an open circuit due to -vely biased.





v 0 The load current flows through D, and the voltage drop across R, will be equal to the if voltage 0 D, forward (replaced by S.C.) N biased 9 0 BO-6 Vo 6 0 0 0 Vin T1 6 5 12 **C**-**C**-Reverse **C**= Biased (replaced by O.C.) 0-0-R For -ve half cycle : 0 0-For -ve half cycle, diocle D<sub>1</sub> is rieversed biased and while diode D<sub>2</sub> is forward biased, hence P<sub>1</sub> is replaced by O.C. & D<sub>2</sub> is replaced by S-C The load current flow through D<sub>2</sub> and the Voltage drop across R<sub>1</sub> is equal to ifp voltage. 0 0 0 0 9 12 0 Vm 0 20 0 No 0 Vin 0 0 0 0 0 R 9



i) Average Voltage:  $V_{dc} = T_{dc}R_{L} =$   $i = V_{dc} = \frac{1}{\sqrt{2}}$   $i = \frac{1}{\sqrt{2}}$   $i = \frac{1}{\sqrt{2}}$ PAGE NO. : 22 DATE : / /  $V_{dc} = T_{dc}R_L = \frac{2T_m}{\pi}R_L$ where Im = Vm Rs+Rf+R, Vdc = 2. Vm RL TT (Rs + Ry + RL)  $T = \frac{1}{(Rst R_{f}) < CR}$   $V_{dC} = \frac{2Vm}{\pi}$   $V_{dC} = \frac{2Vm}{\pi}$   $V_{dC} = \frac{2Vm}{\pi}$   $T_{av} = \frac{1}{2\pi} \int_{0}^{\pi}$   $= \frac{Tm}{2\pi} \int_{0}^{\pi}$   $= \frac{Tm}{2\pi} \int_{0}^{\pi}$  $T \neq (R_{st} R_{f}) < < R_{L}$  $V_{dc} = \frac{2V_m}{\pi} = 0.637V_m$  $T_{av} = \frac{1}{2\pi} \int_{0}^{2\pi} \frac{d\theta}{d\theta} = \frac{1}{2\pi} \int_{0}^{2\pi} \frac{1}{2\pi} \int_{0}^{2\pi} \frac{d\theta}{d\theta} = \frac{1}{2\pi} \int_{0}^{2\pi} \frac{1}{2\pi} \int_{0}^{2\pi} \frac{1}{2\pi} \frac{d\theta}{d\theta} = \frac{1}{2\pi} \int_{0}^{2\pi} \frac{1}{2\pi} \frac{1}{2\pi} \int_{0}^{2\pi} \frac{1}{2\pi} \frac{1}{$  $\int_{0}^{\Pi} \sin \theta \, d\theta - \int_{\Pi}^{2\Pi} \sin \theta \, d\theta$  $= \frac{Im}{2\pi} \left[ (-2)(-2) \right]$  $= \frac{Im}{2\pi} (+4) = \frac{2Jm}{TT} = 0.637 Im,$ --0 -0 Idc = 0.637 Im -0 -



RMS Voltage -: 3 Vgims 2  $\sqrt{\frac{1}{\sqrt{2}}}d(\theta)$ 21 (Vm Sin20 do) 1 217 ] 2 on solving, we get Vamsz Vm Vz (4) RMS Curvent-Igns = 2.Im 3 Peak Factor -Peak Value = Ims Value Vm 7 2 Vm/2 6 Furm Factor -= <u>RMS Value</u> <u>Average Value</u> Form Factor = 1.11 Vm/ 52 2Vm/11



P Ripple Factor -Y = Y = 24 DATE (Imms)<sup>2</sup> Idc)<sup>2</sup> 0 Irms = Im 8 Ipt = 2 Im S  $\left(\frac{\mathrm{Im}}{\mathrm{J2}}/\frac{2\mathrm{Im}}{\mathrm{P}}\right)^{2}$ YFWR = -0 0.483 η = <u>O/P Power</u> × 100 i/p Power = Pdc x100 Pac Pdc = Idc ·RL = (2 . Im) · RL Pac = Imms (Ry+Rs+R)  $= \left(\frac{\mathrm{Im}}{\mathrm{SL}}\right)^2 \left(\mathrm{R}_{\mathrm{f}} + \mathrm{R}_{\mathrm{S}} + \mathrm{R}_{\mathrm{L}}\right)$ Im . 4 . RL 1)2 . RL  $\frac{1}{12} \frac{(R_{f} + R_{s}) < cR_{f}}{\frac{1}{12} \frac{2}{1} \frac{8}{12} \frac{2}{1} \frac{0.812 = 81.23}{2}$ Image (Ry + Rs+Rc)



C C 9 TUF = Pdc C Pac(sated) C C Since both winding are used TUFFOR = 2TUFFOR 1  $= 2 \times 0.287 = 0.574$ C C 10 Peak Inverse Voltage (PIV) -1 C that a diale can withstand without destroying the C C Junction. C PIV= 2Vn C C С Advantages -DUDA X100 0 1) Ripple factor = 0.482 (against 1.21 for HWR) C 0 2) Rectification efficiency is 0.812 or 81.27. D 0 3) Better TUF (secondary) is 0.574 0 0 4) No core saturation problem C Disadvantages -0 0 1) Requises center tapped transformer. G. . G 100 + 8 + 8 0.0



19 26 Bridge Rectifier--0 Main advantage of this bridge circuit 19 is that it does not require a special center tapped transformer, hence reducing its size and cost 0 0 19 **S** 1 0 21-P, V, T 211 0 -0 0 For - ve half cyck The four diode P, R, D, & R, are avanged insucha way that B, D, & P, D, work together. -0 -0 During +ve half cycle of supply, diode D, & D. Conducts ie are replaced by short circuit while diades D3& D4 are reversibilities and is are replaced by Open circuit. ~ -0 -0 0 For -ve half cycle of supply, diode D3 & Dy Conduct while D, & D2 are reverse biased, (OFF). 10 Ripple Foctor Y=0.482 Average Current Ide 2 2 In 5 99 Rechification eff- 7- 0.812 RHS wovent Jams 2 Jm -0 DColi voltage (no. loud) - Vn - 2Vm -0



Zener Diode- highly doped diodes. PAGE NO. : 27 It is a special type of cliocle designed to reliably allow coverent to backwards when a certain set reverse voltage known as Zener Voltage is reached. Zener diades are used for voltage regulation \* It conducts in both discections \* when a large reverse curvent flows, zener diade will not damage. Breakdown Voltage at which the breakdown of P-N Junction diocle occu It depends on the width of the depletion region which in turn depends on doping level. Two mechanisms by which beeak down can occur ar 1) Avalanche Breakdows @ zenenbueakdown



V PAGE NO.: 28 DATE: / 10 Avalanche breakdown- (Avalanche Kultiplication) 0 1) It occurs in a diade which is lightly moderately doped and has thick Junction (depletion 0 layer width is high). It occurs under scoverse biased 1 condition TI occurs when we apply a high sceverse voltage across the diode Chighes than the zener breakdown Voltage (6v) 15v) -■ 3 It occurs be cause of the ionisation of e-shole pair. Astochem a reverse voltage is applied is increased. their is a suise in temperature across the Junction -Due to this vibration of atoms 1 and thus reduces the mean free path for e. Hence Breakdown voltage increases with increase in temperature DIt is +ve temperature coefficient -0 -0 (3) The minopity carriers, under severse biased conditions, flowing through the Junction acquirea -0 K.E which increases with the increase in severse -0 voltage. At high valtages, the KE of ninoguity carriers -0 -0 increases to a level that it knock out e from covalent bonds of servicenductor material. This is a chain reaction and it goeson like this. Hence .... the level of current increases 5 5 -0 -0 IS DEFAD LIVESING гаде ээ



PAGE NO. C DATE С Zener Breakdown-C It occurs due to heavy deping and C have have junction Valence e- which break free under the influence C of applied electric field can be accelerated enough C due to which it distocate the free e from valence 0 to Conduction Band, resulting to a lange number 5 Band of free minority carriers which suddenly increase the reverse current. C C 0 \* It occurs for low Value of reverse Voltage (<6V) C \* When neverse voltage a cross depletion layer increases the thickness of layer (t) increases. С C t ~ V (where Vis applied servese C Voltage) C. 0. \* Let Electric field intensity (E) inside depletion layer Q. 0 C. Q. EXY a R O. EavV The high electric field intensity causes field emissions of e forom immobile sous of depletion layer. I creates a large no. of e - hole pairs inside depletion layer. The external battery forces towards N-region and holes toward P-region. Page 36 **EE DEPARTMENT** 





PAGE NO. 30 So a large reverse current flows from N to Pregion. This phenomenon is Known as zener breakdown After breakdown the reverse current is independent of applied voltage and limited only by external resistance Circuits of 1p without distorting the remaining Al Wareform Classification. clussification-I Classification-I Parallel Positive Negati a) Unbiased a) Unbiased b) Biased b) Brased a) Bias Combined a) Biasod b) Un bio b) Unbiased



9999 classification - I On the basis of oguentation of diode T 0 a) Series Clippenswhen a diode is connected C in series with the load. C C W Unbiased Servies clipper cuts the complete + re C or -ve half. C C C C Vi C RL Vo 0 0 0 0 C and is supplaced by S. closed switch, for +ve half cycle of ifr wave. C For the half C C S S Applying KVL in ilp loop 6 D C Vo= Vi Vi T Page 39 **EE DEPARTMENT** 



For Negative half cycle. Diode is reverse biased and is suplaced by an open circuit. Hence the circuit is as below. V. 10-02 0 BE V0=0 RL op loop Applying KVL in the as i= 0 V0= 0 Transfer characteristrics. Variation of ofp voltage with i/p voltage I/ Vi>0, Vo=Vi Vo=C Vico, Vozo Vot V.= Final Waveform V 21 0 Vn Varov 1211 + wt 0 Forthe hall



(2) Blased Series Clippers. It clips only a portion of wave Ceither + ve on - vehalf It contains a services battery in services with the diode. 211 -Vm For +ve half cycle the diode D is forward biased and is suplaced by S.C. The circuit becomes (V + V. R D 17 Applying KVL at the ofplook. VozVi+V When Vi= OV ; Voz V volls EE DEPARTMENT -- Hence the off waveform obtained is shown above Page 41



9 PAGE NO. :34 DATE: 7 / 0 For Negative Lycle: Diode D will be forward biased till Vi+V is greater than cut in Valtage of diode. ie Vi 4 V, Dis F·B; Vi>V, Dis R·B For ideal diode cut in Voltage is Zero. 9 9 1 -9 When Vi <V, Didde D is forward biased -9 Vo=(-Vi+V) Volto .... Let V= 5V, Vizo 6 Let Vizov Voz 0+5=50 0 V1-21 V V0 = -1+5= 4V 6 V:= 2V Vo=-2+5=3V 4 Vi23V Voz -3+5=2V -V-= 4V Vo= -4+5=1V -V== 5V Vo= -5+5=0V 0 For Vi>V, Diode is reverse biased 6 0 Hence Voz OV. 0 The of P waveform is 0 0 2 V WIN AS VICU. 2 D Yu=0 2 D 21 D D VicV Final waveform 0 (V+Vm) 2 V 0 D n 211 10



35 C C b) Pagallel Clipper-Diode is connected in parallel C to load. Ç (1) Unbiased parallel clipper-Fither complete -ve Or the half cycles are completely clipped off. C 0 C C RS C C D C ZHA Ô C 0 For the half cycle : G RS 0 0 Fon+ve half cycle diode (D) is F. B hence V; 0 D V replaced by s. c 0 IT 0 0 lesand vallay RS Hence the 4 across the shorted terminal is zero. 10=0 9 V020 -0 Hence of waveform 4 Vo 4 0 0 Π 9



PAGE NO 36 9 0 For -ve half yele Diode (Dis sceversed biased and hence 0 it is replaced by open circuit. 9 1 Rs Vo Applying KVL, 1 m Vo=Vi -D 201 -17 --0 -0 C Biased Parallel Clipper -: Clipped off either from +vehalf or -vehalf eyele. A DC battery is connected in series with Diode which is connected in parallel to load. -0 Applying KVC in the op Hence the of wavefor is shown with the C For +ve half cycle For complete + ve half cycle diode is forward biased Vo and is supplaced by S.C. Rs D V η Hence the ofp waveform obtained is shown with the circuit.



PAGE NO : 37 For -vehalf cycle -RS Ra D 211 Voz-V VoeVa when (Vi+V)>0 when (V,+V)<0 For the case of -ve half cycle diode D is forward biased till Vi<V. Hence ofp (for VICV) Voz-V For VizV abde Dis in switching state. For Vi7V. Diode D is completely oreverse biased and the ofp will follow the input ie VozVi Hence the of waveform obtained is V, 217 0 V, 1211 0 VitV -V + Voe + suitching State. -Vm



PAGE NO 38 19 classification-I 10 to clip of or -ve position of alternating -15 coveplete + ve ball a Positive Clippenclips off 19 wair 9 1) Unbiased the clipper--0 clips off complete + ve half & 6 is is unaffected negative 6 -Unbiased basalle as given in Same --2) Blased + ve clippen -0 clips off only a portion of the value 0 Keeping negative half cycle unaffect While 0 0 A DC Battery is connected in series with the dirache 0 0 For +vehalf cycle -0 Vm When Vic V, Diode Dis 0 D. reversed biased The circuit can be sedon RS as. Applying KVI along the loop D to Vi Vi \*



For Vi 2V diode D is forward biased and is replaced by short circuit or closed Switch RS Applying KVLin Offloop un Vo=V Vo=V Hence the of wavefarm is VIZV ViLV Vrz Negative half cycle-Diode is reverse biased for complete -ve half cycle Applying Kur VorV, Vor Vi 20 Hence the ofi waveform is Π 2/1 The final of coureform obtained is 0 wt \_V-



9 DATE S b) Negative clippenclips off the negative position of 8 6 wave -O Unbiased -ve clippen -8 complete - ve half of wave is ve half remain unchanged. 8 0 cut 6 Example Half wave Rectifier 0 6 © Biased Negative clipper-Bottery is connected in series 0 with the diode 9 0 Rs Far + ve half ycle ٢ Vi D Vo The dipole D is reversed biased Ø for complete +ve half cyc Ø and the off will the follow 0 0 ilp. Rs RJ 0 4 0 12 0 V 0 Ø 0 Applying KVL in the loop D 9 Vo= Vi Vi Ð Vm D Hence the opwaveforms Put Ø **EE DEPARTMENT** Page 48



For -vehalf cycle -For Wil < IV), didde Dis scenersed biased. The ckt is shown below. R Hence Vo=Vi D Vo=V, For IV, I>, IVI, diode D, is forward biased. The clet is shown below : RS O/P valtage is constant and equal to voltage of ballery (ie - V) Vo=-Vo Hence the ofp wave form П 21 wit -V Final of waveform Vh 20 D wt -v.



c) Combined Positive and Negative Clipper : Batteries of opposite polarities are connected in parallel Diode P. & D. are included in services with the batteries. Souch that Rs M vr V.  $D_{2}$ Di TV2 Vo VI For +ve half cycle - Diocle Dz is reversed biased for whole + ve half cycle. Diode D, is also reverse biased for Vi < Vi, Diode D, will be replaced by open iscuit RJ Applying KVL 0, 20 Vo=Vi V, Vo=Vi ٧, √, For  $V_i \ge V_i$ , diode D, is forward biased and is replaced by short circuit ::  $V_0 = V_i$ V. twt 17 O



43 PAGE NO .: DATE For -ve half cycle -For 14:1<1/21 Diode D, is suverse biased for whole -ve cycle Diode D2 is suverse biased till V-<V2, hence replaced by open circuit. Rs Hence of P voltage w Vo=V; VozVi - V2 + -T-For IVUI>IV,1 Dz is forward biased and D, is reversed biased. RS NO 0,0 D VI Vo 2 - V2 Ū 1210 VL -12 S. Hence the overall waveform V, 21) 0 wt -V2 **EE DEPARTMENT** Page 51



PAGE NO. 44 Clamping Circuits -De level without clipping. It must have a capacitor, a diode, a resistive element. It can also have DC battery source. \* The time constan (RC) of circuit should be high enough to ensure that voltage across capacitor does not change significantly when diode is reversed biased a) Positive clamper adding the DC component. This result in suising of the level of Signal. +Vm Negative half Cycle - Diode Dis F.B and due to which Capaciton Charges to voltage level Vm with polarity P  $\gamma_{i}$ For this case the capacitor gets charged to Max. (Vm)



Hence Vo = O volts for (only for first cycle Outzoto 13) For Positive Half cycle -! It is assumed that the charge across apacitos remains the same. Diode Pis reverse biased for this case and hence is suplaced by O.C. Rt Voz VitVm D С С Applying KVL across the loop C C Vo= Vi+Vm C o For next -ve half cycle, due to charge across Capacitor, Diode Dwill prow always be reverse biased and hence is replaced by O.C. C 9 Q 4 · Vo = Vi+Vm 0 C Mence the output Waveform is 0 Q 0 20 30 T 5



PAGE NO : 46 DATE Vo Vo 2Vm 21-Vm Vm ON 0 21) D 317 217 0 Ħ wt > (shifted Waveform) ( Osiginal Waveform) shown in book. Negative Clamper -Clamps the AC signal to a lower level **√**i HC **\*** 20 3 20 at 0 0 0 0 0 0 0 Vin For +ve half cycle --0 Vm Diode D is forward biased s cerpacitor charges to Vm with the shown palaecity. Pc + V6=0 0 RS D ViG 2 L Ø For -ve half cycle : 9 Diode Dis seeverse biased and is D suplaced by open circuit 2 D Voz Vi-Vm 1 0



47 PAGE NO. Im 11+ D = Vi-Vn RL C C In this the of voltage is lowered by amount -Vm C C C à \$ С 0 211 С Wb С C 0 (3) Biased Clappers ; 0 0 When a battery is included in series with the 0 0 9  $^{++}$ 9 V, D 4 F 9 9 For -ve half cycle. Diode Dis forward biased and the capacitor c charges to voltage (Vm+E). 9 9 00 -



5 FAGE NO : 48 (Vm+E) DATE -11--D 1 + Vo=E 1 E -0 1 -1 For +ve half cycle --Diode Dis suevere biased -Applying KVLinloop Yoz Vi+Vm+E 0 0 -Vm+E-0 -11-0 Vn V0= Vi+Vm+E - 3 2 211 П 0 E -0 Hence the of waveform obtained ٢ ۲ 0 (E+Vm) 0 E 0 0 wt D 20 31 0 0 Ø Ø D D 0 D 10