Jaipur Engineering College and Research Center

Department of Artificial Intelligence and Data Science

Virtual Lab

Semester III, Session 2021-2022

Data Structures and Algorithms Lab:

Exp No.	Title of the Experiment	Virtual Lab Link
1	Implementation of polynomial with linked list	https://cse01-iiith.vlabs.ac.in/exp/polynomials/
2	Expression evaluation with stack	https://cse01-iiith.vlabs.ac.in/exp/expression-evaluation/
3	Sorting using Array	https://cse01-iiith.vlabs.ac.in/exp/sorting/
4	Search Tree	https://cse01-iiith.vlabs.ac.in/exp/search-trees/

Object Oriented Programming Lab:

Exp No.	Title of the Experiment	Virtual Lab Link
1.	Class and object concept	http://vlabs.iitb.ac.in/vlabs-dev/labs/oops/labs/exp2/index.php
2	Understand constructor	http://vlabs.iitb.ac.in/vlabs-dev/labs/oops/labs/exp5/index.php
3	Understand Function overloading	http://vlabs.iitb.ac.in/vlabs-dev/labs/oops/labs/exp4/index.php
4	Understand Inheritance	http://vlabs.iitb.ac.in/vlabs-dev/labs/oops/labs/exp1/index.php

Software Engineering Lab:

Exp No.	Title of the Experiment	Virtual Lab Link
1	COCOMO Model	http://vlabs.iitkgp.ernet.in/se/2/
2	Understand Data Flow Diagram	http://vlabs.iitkgp.ernet.in/se/8/
3	Develop Software Requirements Specification (SRS) for a given problem in IEEE template.	http://vlabs.iitkgp.ernet.in/se/

Digital Electronics Lab

Exp No.	Title of the Experiment	Virtual Lab Link
1.	Verification and implementation of logic gates: AND, OR, NOR, NAND, NOR, Ex-OR, Ex-NOR	https://de-iitr.vlabs.ac.in/exp/truth-table-gates/
2	Verification of the truth table of half adder and full adder by using XOR and NAND gates respectively	https://de-iitr.vlabs.ac.in/exp/half-full-adder/
3	Implementation of the logic functions i.e. AND, OR, NOT, Ex-OR, Ex- NOR with the help of NAND and NOR gates respectively.	https://de-iitr.vlabs.ac.in/exp/realization-of-logic-functions/
4	Verification of truth table of RS, JK, T and D flip-flops	https://de-iitr.vlabs.ac.in/exp/truth-tables-flip-flops/
5	Analyse the truth table of 4-bit SIPO shift register	https://de-iitr.vlabs.ac.in/exp/4bit-sipo-shift-register/
6	Analyse the truth table and working of 1x4 De-Multiplexer and 4x1 Multiplexer	https://de-iitr.vlabs.ac.in/exp/multiplexer-demultiplexer/
7	Verify the truth table and timing diagram of 4-bit synchronous parallel counter and 4-bit asynchronous parallel counter by using JK flip flop	https://de-iitr.vlabs.ac.in/exp/4bit-synchronous-asynchronous-counter/
8	Analyse the truth table of binary to gray and gray to binary converter	https://de-iitr.vlabs.ac.in/exp/binary-conversion/