

A Certificate Program

On

VLSI Design

From 10th July to 18th July, 2018

**Conducted by Techienest India Pvt. Ltd.,
Jaipur**

Organised By



**JAIPUR ENGINEERING COLLEGE
AND RESEARCH CENTRE**

**Department of Electronics and Communication
Engineering**

**Jaipur Engineering College and Research
Centre, Jaipur**



Jaipur Engineering College and Research Centre, Jaipur
Department of Electronics and Communication Engineering

Minutes of Meeting

Date: July 05, 2018

A Meeting of faculty members involved in SD Cell was held on July 05, 2018 at 1:00 pm to discuss the Introduction of new Certificate Courses for students to bridge the Industry-Institute gap.

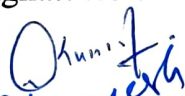

The details of the new certificate program would be as follows:

Name of the Program: VLSI Design

Duration: 10/07/2018 to 18/07/2018.

In Collaboration with: Techienest India Pvt. Ltd., Jaipur

Signatures of Faculty Members:

1. 
2. 



JAIPUR ENGINEERING COLLEGE AND RESEARCH CENTRE
Department of Electronics and Communication Engineering

To,
The Principal,
JECRC, Jaipur

Date: 06/07/2018

Subject: Proposal for Certificate Course.

Respected sir,

It is to bring to your kind notice that students of ECE, 2nd and 3rd year approached us and requested to conduct a certificate program for them on **VLSI Design**. In this regard, we hereby request you to approve the Certificate Course as under.

Conducted By: Techienest India Private Limited.

Topic: VLSI Design

Target: Second year students and third year student

Organizer: Mr. Ashutosh Sharma, (SDO) ECE Department


Objective of the Program: The Main objective of this **Program** is to make the students **conceptually and practically aware** about:

- Get Hands on Training on System Verilog in Industry Standard EDA flow.
- Advanced Front End Design & Verification
- Verification Methodologies- OVM, UVM- Overview
- System Verilog Class Based approach

Topics and hands-on activity in the Program:

- Hands-on Sessions Advanced Front End Design & Verification
- Hands-on -Introduction to System Verilog & OOPS Concept
- Understanding System Verilog Class Based approach
- Monitors, Checkers, Scoreboards, Introduction to Verification Methodologies- OVM, UVM

You are requested to approve the above.


With Regards
HOD (ECE)

Head of the Department
Electronics & Communication Engineering
JECRC, Jaipur

Objective of the Workshop: The Main objective of this VLSI workshop is to make the students conceptually and practically aware about:

- Get Hands on Training on System Verilog in Industry Standard EDA flow.
- Advanced Front End Design & Verification
- Verification Methodologies- OVM, UVM- Overview
- System Verilog Class Based approach

Topic: VLSI Design.

Course Fee: Free of Cost

How to Apply: Contact Mr. Ashutosh Sharma, AP (ECE)

Target: Second year students and third year student

Duration: 45 hrs (10/07/2018 to 18/07/2018)

Organizer: Mr. Ashutosh Sharma, AP (ECE)

Topics and hands-on activity in the workshop:

- Hands-on Sessions Advanced Front End Design & Verification
- Hands-on -Introduction to System Verilog & OOPS Concept
- Understanding System Verilog Class Based approach
- Monitors, Checkers, Scoreboards, Introduction to Verification Methodologies- OVM, UVM
- Final Concluding Remarks

A

**Certificate Program
On**

VLSI Design

From 10th July to 18th July, 2018

Conducted by: Techniest India Pvt. Ltd.,

Jaipur

Organised By:



**JAIPUR ENGINEERING COLLEGE
AND RESEARCH CENTRE**

**Department of Electronics and Communication Engineering
Jaipur Engineering College and Research Centre, Jaipur**

Index

Sr. No.	Contents
1	MOU
2	Course Curriculum
3	Attendance Sheet
4	Feedback
5	Certificate (Photocopy)

Signature
SDO - RCE
Jaipur Engineering College and Research Centre
JAIPUR

Memorandum of Understanding

Is executed on 12th October, 2018

between

TechieNest Pvt. Ltd., hereinafter referred to as "TechieNest", A company duly incorporated under the provisions of Companies Act 1956, having its registered office at 7 Jawahar Nagar Colony, Gate No 1, near Glass Factory, Tonk Road, Jaipur - 302015 represented through its authorised signatory Mr Chandra Bhan, party of the first part.

And

Jaipur Engineering College & Research Centre, hereinafter referred as "JECRC, Jaipur" represented through its, Principal Dr Vinay Kumar Chandana, party of the second part

For

Collaboration of Training/workshops/Seminar/Projects is for the 3 years w.e.f. 12th October 2018.

TechieNest Pvt. Ltd., Jaipur DELIVERABLES:

1. TechieNest will sponsor INR 1 lakh per year in two instalment.
2. TechieNest will run all technical courses for Electrical & Electronics branch.
3. TechieNest will set up a centre of Excellence in Embedded Systems at JECRC campus.
4. TechieNest will set up training kit in excellence centre (Refundable after training).
5. Students will trained to participate in national level events.
6. The cost of training will be discussed before the start of training course/ making any announcement to the students.
7. 100 % Placement Assistance to each Participants/ Students who will complete minimum three trainings from us.
8. Lifetime Free of cost hands on practice membership card to each participants.
9. A Chance to each participant to win TechieNest Scholarship for any future training on behalf of final training assessment test.
10. Golden opportunity to do summer internship as TechieNest Research Intern at one of our 7 offices across India.
11. TechieNest will provide Certificate to each Student Coordinator.
12. TechieNest will provide participation Certificate to each participants.
13. TechieNest will provide letter of appreciation to college and faculty coordinators.
14. TechieNest will help students to organize technical fest/event.

V. Chandana
PRINCIPAL
Jaipur Engineering College &
Research Center
Tonk Road, Jaipur - 303 905

For TechieNest Private Limited
Director


JECRC, Jaipur DELIVERABLES:

1. JECRC will arrange in house training for EC and electrical branch on regular basis.
2. Provide following technical requirements for setting Excellence Centre: -
 - A room.
 - 1 projector
 - White board and marker
 - Extension board (for power supply)
3. Assign at least 2 faculty coordinators from each branch who will support from starting to end of the training.
4. Arrange seminars to interact with students.
5. Try to get maximum registration for Training.
6. Provide Association Certificate/Momentous to TechieNest.
7. TechieNest logo and name will be placed in JECRC website and all social media pages.
8. TechieNest Poster, banner, standee in respective branches.
9. TechieNest name, logo, banner, canopy during annual fest/conference of college.

Terms & Condition

1. Second party will not collaborate/invite any other company/institute/Member for EC and electrical branch and during college fest.

Signature on Behalf JECRC, JAIPUR




Name: Dr Vinay Kumar Chandana
Title: Principal
JECRC, JAIPUR
Date: _____

PRINCIPAL
Jaipur Engineering College &
Research Center.
Tonk Road, Jaipur - 303 905

Signature on Behalf of TechieNest Pvt Ltd, Jaipur

For Techiest Private Limited


Director

Name: Chandra Bhan
Title: Director
TechieNest Pvt Ltd, Jaipur
Date: _____



Course Curriculum of the Certificate Program on VLSI Design

Duration: 8 Days (10/07/2018 to 18/07/2018)

No. of students attended: 125

Introduction to VLSI Technology:

Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining hundreds of thousands of transistors or devices into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. Before the introduction of VLSI technology most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. VLSI lets IC designers add all of these into one chip.

The first semiconductor chips held two transistors each. Subsequent advances added more transistors, and as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device. Now known retrospectively as *small-scale integration* (SSI), improvements in technique led to devices with hundreds of logic gates, known as *medium-scale integration* (MSI). Further improvements led to *large-scale integration* (LSI), i.e. systems with at least a thousand logic gates. Current technology has moved far past this mark and today's microprocessors have many millions of gates and billions of individual transistors.

At one time, there was an effort to name and calibrate various levels of large-scale integration above VLSI. Terms like *ultra-large-scale integration* (ULSI) were used. But the huge number of gates and transistors available on common devices has rendered such fine distinctions moot. Terms suggesting greater than VLSI levels of integration are no longer in widespread use.

In 2008, billion-transistor processors became commercially available. This became more commonplace as semiconductor fabrication advanced from the

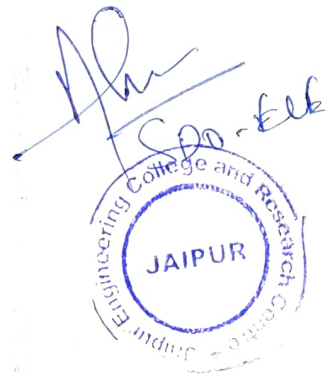
then-current generation of 65 nm processes. Current designs, unlike the earliest devices, use extensive design automation and automated logic synthesis to lay out the transistors, enabling higher levels of complexity in the resulting logic functionality. Certain high-performance logic blocks like the SRAM (static random-access memory) cell, are still designed by hand to ensure the highest efficiency.

Objective of the Workshop: The Main objective of this VLSI workshop is to make the students **conceptually and practically** aware about:

- Get Hands on Training on SystemVerilog in Industry Standard EDA flow.
- Advanced Front End Design & Verification
- Verification Methodologies- OVM, UVM- Overview
- System Verilog Class Based approach

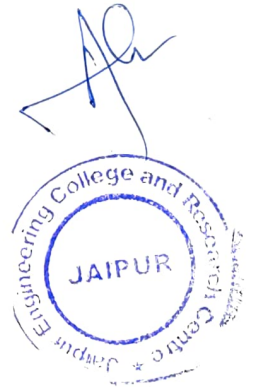
Topics and hands-on activity in the workshop:

- Hands-on Sessions Advanced Front End Design & Verification
- Hands-on -Introduction to System Verilog & OOPS Concept
- Understanding System Verilog Class Based approach
- Monitors, Checkers, Scoreboards, Introduction to Verification Methodologies- OVM, UVM
- Final Concluding Remarks

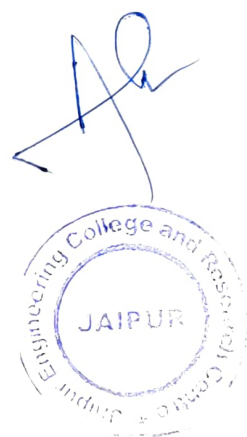


Name of the Participants

1	17EJCEC128	NIKHIL SOMANI
2	17EJCEC129	NISHANT PAHWA
3	17EJCEC130	NITESH RAM KISHORE MINA
4	17EJCEC131	NITIN KUMAR
5	17EJCEC132	NITIN NIRWAN
6	17EJCEC133	OJASV SHARMA
7	17EJCEC134	PANKAJ AGARWAL
8	17EJCEC135	PANKAJ JANGID
9	17EJCEC136	PANKAJ JOSHI
10	17EJCEC137	PANKAJ SHARMA
11	17EJCEC138	PRACHI CHAUHAN
12	17EJCEC139	PRANAY KASLIWAL
13	17EJCEC140	PRANSHU CHAURASIA
14	17EJCEC141	PRANSHU SHARMA
15	17EJCEC142	PRATEEK KUMAR
16	17EJCEC143	PRATEEK KUMAR MISHRA
17	17EJCEC144	PRATEEK SHARMA
18	17EJCEC145	PRAVEEN SHARMA
19	17EJCEC146	PRIYA LADDHA
20	17EJCEC147	PRIYAL AGARWAL
21	17EJCEC148	PRIYANSHI KHANDELWAL
22	17EJCEC149	PURVA BANTHIA
23	17EJCEC150	PUSHPENDRA SONI
24	17EJCEC151	RAGHAV DAS SINGHAL
25	17EJCEC152	RAGHAV SINGHAL
26	17EJCEC153	RAGHAVENDRA KUMAR THAKUR
27	17EJCEC155	RAHUL BALODA
28	17EJCEC156	RAHUL KUMAR DUBEY
29	17EJCEC157	RAHUL SOGANI
30	17EJCEC158	RAJAN DHAWAN
31	17EJCEC159	RAJAT MUNDRA
32	17EJCEC160	RAJAT PUROHIT
33	17EJCEC161	RAKHI RAWAT
34	17EJCEC162	RAKSHIT SHARMA
35	17EJCEC163	RAMAN GARG
36	17EJCEC164	RAVI NAGAR
37	17EJCEC165	RICHA MISHRA
38	17EJCEC166	RINCY CHACKO KURIEN
39	17EJCEC167	RISHABH JAIN
40	17EJCEC168	RISHABH KHANDELWAL
41	17EJCEC169	RISHI RAJ SHEKHAWAT
42	17EJCEC170	RITIK JAIN




43	17EJCEC171	RIYA KANOONGO
44	17EJCEC172	RIYA SHARMA
45	17EJCEC173	ROHIT ANAND
46	17EJCEC174	ROHIT JANGID
47	17EJCEC175	ROHIT SHARMA
48	17EJCEC176	ROHITASHAV GARG
49	17EJCEC177	RUPAL SAINI
50	17EJCEC178	SAGAR NIGAM
51	17EJCEC179	SAKET SHARMA
52	17EJCEC180	SAKINA SAIFY
53	17EJCEC183	SANSKAR SHARMA
54	17EJCEC184	SARTHAK CHATURVEDI
55	17EJCEC185	SARTHAK SAXENA
56	17EJCEC186	SATYAM KUMAR JHA
57	17EJCEC187	SAURABH GHOSH
58	17EJCEC188	SAURABH KUMAR
59	17EJCEC189	SHAHID ALI
60	17EJCEC190	SHASHI SHEKHAR GAURAV
61	17EJCEC192	SHIVAM SHUKLA
62	17EJCEC193	SHIVANGI SHARMA
63	17EJCEC194	SHIVANSH PANDYA
64	17EJCEC195	SHUBHAM AGARWAL
65	17EJCEC197	SHUBHAM MITTAL
66	17EJCEC198	SHUBHAM RATHI
67	17EJCEC851	SHUBHAM SHARMA
68	17EJCEC852	SHYAM SOMANI
69	17EJCEC853	SIDDHARTH KHARRA
70	17EJCEC855	SOURAV CHHIPA
71	17EJCEC856	SPARSH MEENA
72	17EJCEC857	SUKHBIR SINGH BHACHU
73	17EJCEC858	SURBHI KHANDELWAL
74	17EJCEC859	TANIYA JOSHI
75	17EJCEC860	TANUJ AGARWAL
76	17EJCEC861	TANUSHI AGARWAL
77	17EJCEC863	TEJASWI BANSAL
78	17EJCEC864	TUSHAR SHARMA
79	17EJCEC865	UJJWAL SHARMA
80	17EJCEC866	UPENDRA KUMAR SHARMA
81	17EJCEC867	UTSAV SHARMA
82	17EJCEC868	VAIBHAV AGARWAL
83	17EJCEC869	VAIBHAV MAHESHWARI
84	17EJCEC870	VARDAAN BHALLA
85	17EJCEC872	VIDUSHI MANGNANI
86	17EJCEC873	VINESH GUPTA
87	17EJCEC874	VINIT SINGH

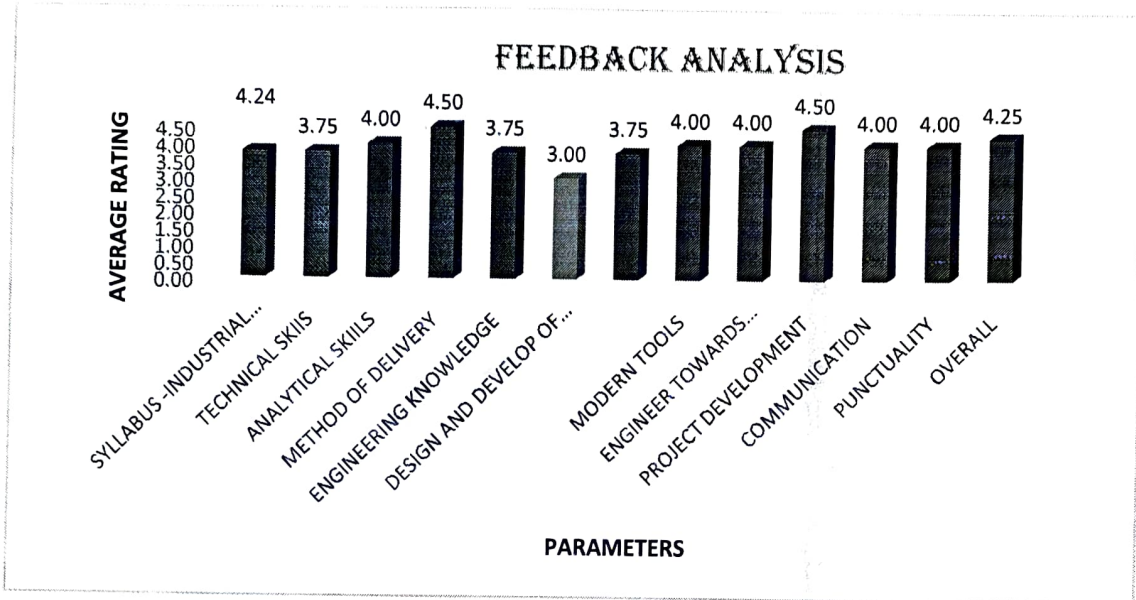


88	17EJCEC875	VIPIN AANJANA
89	17EJCEC876	VIPUL GWALA
90	17EJCEC877	VIRENDRA SINGH
91	17EJCEC879	VISHWASH KHANDAL
92	17EJCEC880	VIVEK PANDEY
93	17EJCEC881	YAMAN PAREEK
94	17EJCEC882	YASH DIXIT
95	17EJCEC883	YASH GUPTA
96	17EJCEC884	YASH GUPTA
97	17EJCEC885	YASH SHARMA
98	17EJCEC886	YUVRAJ SINGH BADGUJAR
99	17EJCEC300	CHANDRA SHEKHAR VYAS
100	17EJCEC301	SAURABH SHARMA
101	17EJCEC302	SURYA PRATAP SINGH
102	Diploma	Ranjeet Singh
103	17EJCEC400	Kareena Khan
104	17EJCEC062	DANISH KHAN
105	17EJCEC063	DEEKSHA SINGH
106	17EJCEC064	DEEPAK CHOUDHARY
107	17EJCEC065	DEEPAKSHI JOSHI
108	17EJCEC066	DEEPANSHU GUPTA
109	17EJCEC067	DEEPESH MALHOTRA
110	17EJCEC068	DEEPESH MITTAL
111	17EJCEC069	DEPENDRA SETHIYA
112	17EJCEC070	DEVANG AGARWAL
113	17EJCEC071	DHRUVA SHARMA
114	17EJCEC072	DIVYA TINKAR
115	17EJCEC073	DIVYANSH
116	17EJCEC074	DIVYANSH JADON
117	17EJCEC075	DIVYANSH SINGH
118	17EJCEC077	GANESH GOYAL
119	17EJCEC078	GARVIT SHARMA
120	17EJCEC079	GARVIT SHARMA
121	17EJCEC081	GIRISH MISHRA
122	17EJCEC082	HARDIK GANDHI
123	17EJCEC083	HARDIK SOGANI
124	17EJCEC084	HARENDER SINGH
125	17EJCEC085	HARSH CHHAWAL


 SDO-ef



 Head of the Department
 Electronics & Communication Engineering
 JECRC, Jaipur

Feedback



Handwritten signature
10-06-2024

Engineering College and Research Centre
JAIPUR



JECRC Foundation

JAIPUR ENGINEERING COLLEGE AND RESEARCH CENTRE

Certification Program VLSI Design

Certificate of Participation

This certificate is presented to

OJASV SHARMA

IN RECOGNITION OF PARTICIPATING IN VLSI DESIGN CERTIFICATE PROGRAM, ORGANIZED BY DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING FOR SECOND YEAR STUDENTS. THE DURATION OF THE PROGRAM WAS EIGHT DAYS, I.E., JULY 10th TO 18th JULY 2018. THE STUDENT HAS EXHIBITED EXCELLENT PERFORMANCE DURING THE PROGRAM.

Dr. Lokesh Bansal

HOD

Dept. of ECE

Dr. Vinay K. Chandna

Principal

JECRC



JAIPUR ENGINEERING COLLEGE AND RESEARCH CENTRE

Certification Program VLSI Design
Certificate of Participation

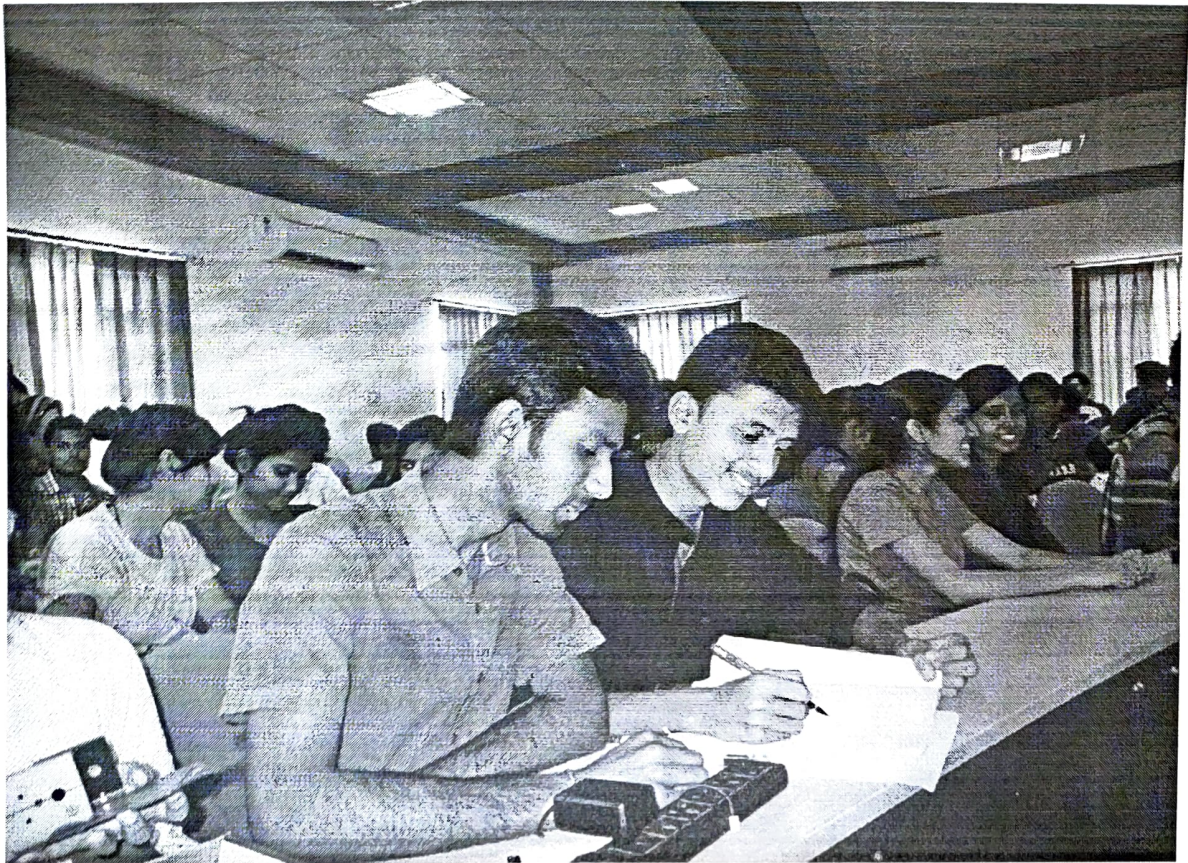
This certificate is presented to

PRACHI CHAUHAN

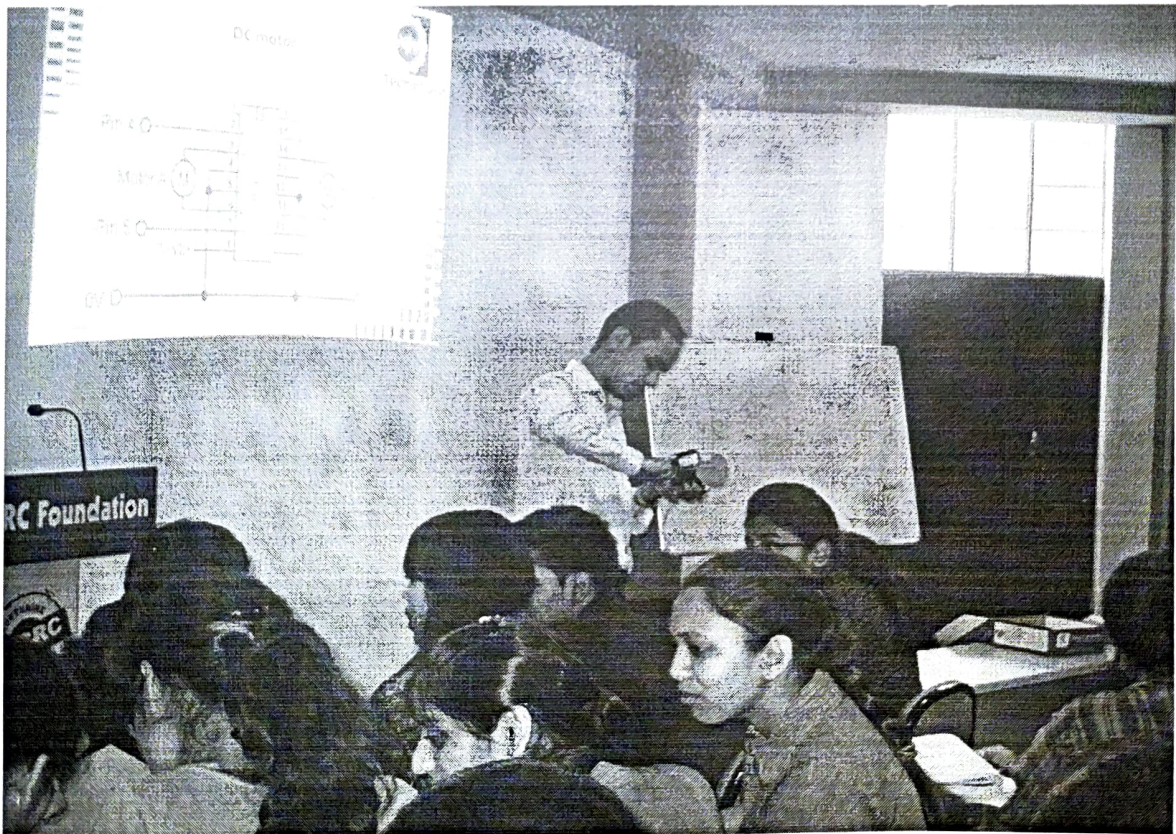
IN RECOGNITION OF PARTICIPATING IN VLSI DESIGN CERTIFICATE PROGRAM, ORGANIZED BY DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING FOR SECOND YEAR STUDENTS. THE DURATION OF THE PROGRAM WAS EIGHT DAYS, I.E., JULY 10th TO 18th JULY 2018. THE STUDENT HAS EXHIBITED EXCELLENT PERFORMANCE DURING THE PROGRAM.

Dr. Lokesh Bansal
HOD
Dept. of ECE

Dr. Vinay K. Chandna
Principal
JECRC



(10/07/2018, Session 1)



(10/07/2018, Session 2)






(12/07/2018, Session 2)



43	RIYA KANOONGO	P	P	P	P	P	P	P	P
44	RIYA SHARMA	P	P	P	P	P	P	P	P
45	ROHIT ANAND	P	A	P	P	P	P	P	P
46	ROHIT JANGID	P	A	P	P	P	P	P	P
47	ROHIT SHARMA	P	A	P	P	P	P	P	P
48	ROHITASHAV GARG	P	P	P	P	P	P	P	P
49	RUPAL SAINI	P	P	P	P	P	P	P	P
50	SAGAR NIGAM	P	P	P	P	P	P	P	P
51	SAKET SHARMA	P	P	P	P	P	P	P	P
52	SAKINA SAIIFY	P	A	P	P	P	P	P	P
53	SANSKAR SHARMA	P	P	P	P	P	P	P	P
54	SARTHAK CHATURVEDI	P	P	P	P	P	P	P	P
55	SARTHAK SAXENA	P	P	P	P	P	P	P	P
56	SATYAM KUMAR JHA	P	A	P	P	P	P	P	P
57	SAURABH GHOSH	P	P	A	P	P	P	P	P
58	SAURABH KUMAR	P	P	P	P	P	P	P	P
59	SHAHID ALI	P	P	P	P	P	P	P	P
60	SHASHI SHEKHAR GAURAV	P	P	P	P	P	P	P	P
61	SHIVAM SHUKLA	P	A	P	P	P	P	A	P
62	SHIVANGI SHARMA	P	P	P	P	P	P	P	A
63	SHIVANSH PANDYA	P	P	P	P	P	P	P	P
64	SHUBHAM AGARWAL	P	P	P	P	P	P	P	P
65	SHUBHAM MITTAL	P	P	P	P	P	P	P	P
66	SHUBHAM RATHI	P	P	A	P	P	P	P	P
67	SHUBHAM SHARMA	P	P	P	P	P	P	P	P
68	SHYAM SOMANI	P	A	P	P	P	P	P	P
69	SIDDHARTH KHARRA	P	P	P	P	P	P	P	P
70	SOURAV CHHIPA	P	P	P	P	P	P	P	P
71	SPARSH MEENA	P	P	P	P	P	P	P	P
72	SUKHBIR SINGH BHACHU	P	P	P	P	P	P	P	P
73	SURBHI KHANDELWAL	P	P	P	P	P	P	P	P
74	TANIYA JOSHI	P	A	P	P	P	P	P	P
75	TANUJ AGARWAL	P	P	P	P	P	P	P	P
76	TANUSHI AGARWAL	P	P	P	P	P	P	P	P
77	TEJASWI BANSAL	P	P	P	P	P	P	P	P
78	TUSHAR SHARMA	P	A	P	P	P	P	P	P
79	UJJWAL SHARMA	P	P	P	P	P	P	P	P
80	UPENDRA KUMAR SHARMA	P	P	P	P	P	P	P	P
81	UTSAV SHARMA	P	P	P	P	P	P	P	P
82	VAIBHAV AGARWAL	P	P	P	P	P	P	P	P
83	VAIBHAV MAHESHWARI	P	P	P	P	P	P	P	A
84	VARDAAN BHALLA	P	P	A	P	P	P	A	P
85	VIDUSHI MANGNANI	P	P	P	P	P	P	P	P
86	VINESH GUPTA	P	P	P	P	P	P	P	P
87	VINIT SINGH	P	A	P	P	P	P	P	P
88	VIPIN AANJANA	P	P	P	P	P	P	P	P
89	VIPUL GWALA	P	P	P	P	P	P	P	P
90	VIRENDRA SINGH	P	P	P	P	P	P	P	P
91	VISHWASH KHANDAL	P	P	P	P	P	P	P	P
92	VIVEK PANDEY	P	P	P	P	P	P	P	P

93	YAMAN PAREEK	P	P	P	P	P	P	P	P
94	YASH DIXIT	P	P	P	P	P	P	P	P
95	YASH GUPTA	P	P	P	P	P	P	P	P
96	YASH GUPTA	P	P	P	P	P	P	P	P
97	YASH SHARMA	P	P	P	P	P	P	P	P
98	YUVRAJ SINGH BADGUJAR	P	A	P	P	P	P	P	P
99	CHANDRA SHEKHAR VYAS	P	P	P	P	P	P	P	P
100	SAURABH SHARMA	P	A	A	P	P	P	P	P
101	SURYA PRATAP SINGH	P	P	P	P	P	P	P	A
102	Ranjeet Singh	P	A	P	P	P	P	P	P
103	Kareena Khan	P	P	P	P	P	P	P	P
104	DANISH KHAN	P	A	P	P	P	P	P	P
105	DEEKSHA SINGH	P	P	P	P	P	P	P	P
106	DEEPAK CHOUDHARY	P	A	P	P	P	P	P	P
107	DEEPAKSHI JOSHI	P	A	P	P	P	P	A	P
108	DEEPANSHU GUPTA	P	A	P	P	P	P	P	P
109	DEEPESH MALHOTRA	P	A	P	P	P	P	P	P
110	DEEPESH MITTAL	P	P	P	P	P	P	P	P
111	DEPENDRA SETHIYA	P	P	P	P	P	P	P	P
112	DEVANG AGARWAL	P	P	P	P	P	P	P	P
113	DHRUVA SHARMA	P	P	P	P	P	P	P	P
114	DIVYA TINKAR	P	P	P	P	P	P	P	P
115	DIVYANSH	P	A	P	P	P	P	P	P
116	DIVYANSH JADON	P	P	P	P	P	P	P	P
117	DIVYANSH SINGH	P	P	P	P	P	P	P	P
118	GANESH GOYAL	P	P	P	P	P	P	P	P
119	GARVIT SHARMA	P	P	P	P	P	P	P	A
120	GARVIT SHARMA	P	P	P	P	P	P	P	P
121	GIRISH MISHRA	P	P	P	P	P	P	P	P
122	HARDIK GANDHI	P	P	P	P	P	P	P	P
123	HARDIK SOGANI	P	P	A	P	P	P	A	P
124	HARENDER SINGH	P	P	P	P	P	P	P	P
125	HARSH CHHAWAL	P	P	P	P	P	P	P	P



 ADD-EEE